PAL – NTSC ENCODER

GENERAL DESCRIPTION

The TDA2501 encodes two colour-difference signals R-Y and B-Y onto one subcarrier. Quadrature modulation allows the coding to be in accordance with either the PAL or NTSC system.

Features

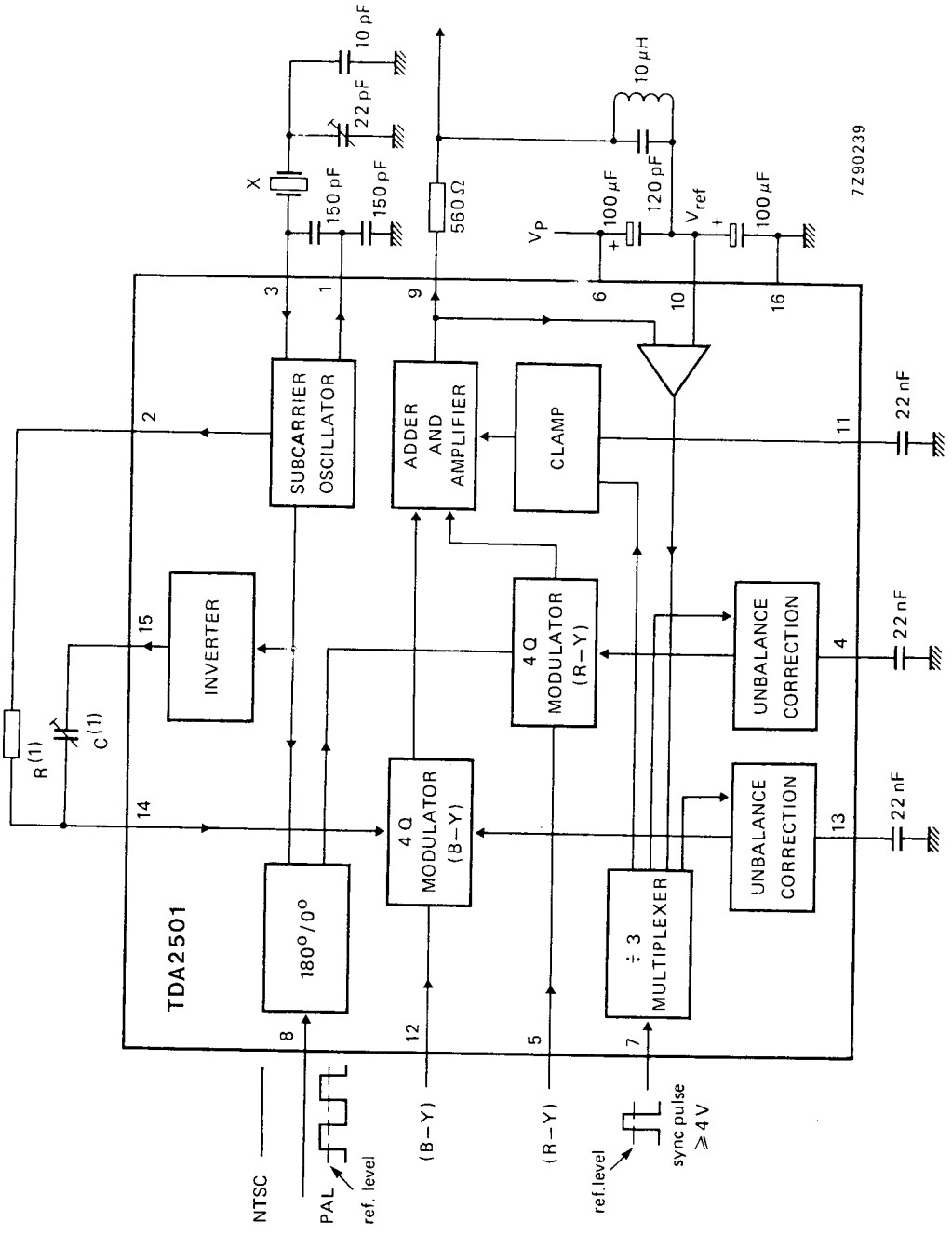
- Generates two sinusoidal subcarriers with a relative phase of 90° (also accepts external subcarriers)
- Modulates the two subcarriers with the colour difference signals
- Inverts the output from one modulator on command of an external signal (as in case of PAL)
- Sums the output from the modulators to obtain a quadrature modulated output signal
- Clamps the output DC level to a reference voltage
- Divides the frequency of horizontal sync pulses by three so that the output level can be clamped and the balance of the two modulators sequentially controlled during the line-blanking minus burst-key period

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6)	V_P	5.5	6.8	10	V
Supply current range (pin 6)	I_P	28	40	64	mA
Chrominance output voltage (pin 9) (peak-to-peak value)	$V_{9(p-p)}$	–	–	1.4	V
Operating ambient temperature range	T_{amb}	−25	–	+70	°C

PACKAGE OUTLINES

TDA2501 : 16-lead DIL; plastic (with internal heat spreader) (SOT38).
TDA2501T: 16-lead mini-pack; plastic (SO16L; SOT162A).



(1) R = 0.885 (2 π fC); for PAL f = 4.433 619 MHz, R = 963 Ω and C = 33 pF.

Fig.1 Block diagram; also test and application diagram.

DESCRIPTION

The colour difference signals B-Y and R-Y with a maximum amplitude of 1.4 volt are to be applied at pin 12 and pin 5. DC-coupling of the input signals is allowed if their DC levels are within specified limits from the DC level at pin 10 (V_{ref}). The following table shows these limits as a function of supply voltage. The table also shows the limits of the reference voltage range as a function of the supply voltage.

supply voltage V_{6-16} (V)	input DC (R-Y) (B-Y) min. (V)*	V_{5-16} V_{12-16} (V) max. (V)**	reference voltage ▲ V_{10-16} (V)		
			min	typ.	max.
5.5	2.4	3.3	2.3	3.0	3.5
6.0	$> V_{ref} - 1.4$ V	3.8	2.4	3.3	3.9
7.0	$> V_{ref} - 1.4$ V	4.8	2.6	4.0	4.7
8.0	$> V_{ref} - 1.4$ V	5.8	2.8	4.8	5.5
9.0	$> V_{ref} - 1.4$ V	6.8	3.0	5.5	6.3
10.0	$> V_{ref} - 1.4$ V	7.8	3.2	6.3	7.1

* Minimum 2.4 V.

** At $V_S - 2.2$ V.

▲ Minimum values at $0.2\ V_S + 1.2$ V.
Typical values without pull-up or pull-down resistor.
Maximum values at $0.8\ V_S - 0.9$ V.

The inputs (B-Y) and (R-Y) should be zero, independent of their (limited) DC-levels, during the line-blanking minus burst-key period (LB – BK). Clamping the output and correcting the out-of-balance of the modulators, is achieved by applying a HIGH level to pin 7 within the (LB–BK) period (e.g. line sync pulse).

Modulation at output:
V_8 = LOW; output = sc x (B-Y) + sc' x (R-Y)
V_8 = HIGH; output = sc x (B-Y) – sc' x (R-Y)
in which sc' = subcarrier
sc = 90° phase-shifted subcarrier to sc' (sc lags).

The bandpass filter at the output suppresses the DC components of the (R-Y) + (B-Y) signal. Luminance (Y) is not processed by this circuit.

Internal subcarrier

The internal subcarrier oscillator is crystal controlled. The oscillator generates a sinewave with low harmonic distortion and an amplitude of about 500 mV peak-to-peak. The amplitude can be changed if necessary with a current input at pin 1. The adjustment range is 0 to 800 mV, with a corresponding current range of +250 to −150 μA.

Phase shift

To obtain a 90° phase-shifted carrier, two low impedance subcarrier outputs are provided, pins 2 and 15, the last being the inverse of the first. Between pins 2 and 15 an external RC combination must be used to obtain the desired 90° shift. The capacitor value must be limited to 33 pF to minimize subcarrier distortion.

The resistor required between pins 2 and 14 is $0.885\ (2\pi fC)$.

External subcarrier

The (B-Y) and (R-Y) signals can also be multiplied with an external subcarrier. In this event the external subcarrier is connected to pin 1. For maximum input impedance at pin 1 $V_3 = V_{16}$ ($Z_{mi} > 1400\ \Omega$). The same RC network generates the 90° phase-shifted subcarrier. For the use of an externally generated subcarrier, applied at pin 14, the DC level must be the same as that of an RC-network generated one.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6 to pin 16)	V_P	–	13.2	V
Total power dissipation	P_{tot}	see Fig.2		W
Operating ambient temperature range	T_{amb}	−25	+70	°C
Storage temperature range	T_{stg}	−55	+150	°C

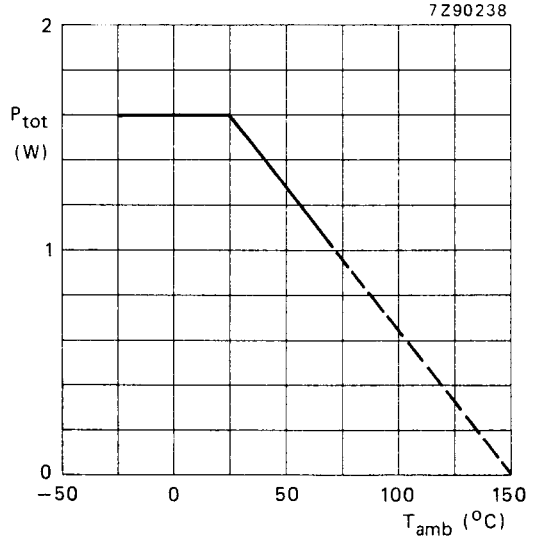


Fig.2 Power derating curve.

CHARACTERISTICS

$V_P = V_{6-10} = -V_{16-10} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Single supply voltage	V_{6-16}	5.5	6.8	10	V
Dual supply voltage					
positive (pin 6)	V_{6-10}	2.0	3.0	5.0	V
negative (pin 16)	$-V_{16-10}$	2.3	3.0	5.0	V
Supply current (pin 10)	I_{10}	−1	0	3.5	mA
positive (pin 6)	I_6	28	40	64	mA
negative (pin 16)	$-I_{16}$	28	40	64	mA
Limitation DC level oscillator feedback	V_1	−30	0	+30	mV
Nominal amplitude input signal (peak-to-peak value)					
pin 5	$V_{5(p-p)}$	–	1	1.4	V
pin 12	$V_{12(p-p)}$	–	1	1.4	V
Input voltages (R-Y) and (B-Y) zero DC level					
pin 5	V_5	2.4	3.3	3.9	V
pin 12	V_{12}	2.4	3.3	3.9	V
Required level of sync input					
HIGH	V_7	4	–	V_P	V
LOW	V_7	–	–	V_{10}	V
Required level of PAL pulse (H/2)					
HIGH	V_8	$V_{10}+0.8$	–	V_P	V
LOW	V_8	$-V_P$	–	0	V
Sync input current $V_7 = V_P + 1$ V	I_7	–	4	15	μA
PAL input current (H/2) $V_8 = V_{10} + 0.8$ V	I_8	–	1.5	5	μA
Chrominance output voltage swing (R-Y) = (B-Y) = 1.4 V; subcarrier pulse = 0.5 V (peak-to-peak value)	$V_{9(p-p)}$	–	–	1.4	V
Amplitude of suppressed subcarrier	V_9	0	7	16	mV
Input currents					
$V_4 = V_{10}$	I_4	0	1.5	5	μA
$V_{11} = V_{10}$	I_{11}	0	1.5	5	μA
$V_{13} = V_{10}$	I_{13}	0	1.5	5	μA
$V_5 = V_{10}$	I_5	0	9	30	μA
$V_{12} = V_{10}$	I_{12}	0	9	30	μA
$V_{14} = V_{16} + 2.3$ V	I_{14}	–	6	–	μA
Input impedance					
(R-Y)	Z_5	–	160	–	kΩ
(B-Y)	Z_{12}	–	160	–	kΩ