

## FEATURES

**Operates from 1.65 V to 3.6 V supply rails**  
**Bidirectional level translation, unidirectional signal path**  
**8-lead SOT-23 and MSOP packages**  
**Bypass or normal operation**  
**Short circuit protection**

## APPLICATIONS

**JTAG chain bypassing**  
**Daisy-chain bypassing**  
**Digital switching**

## FUNCTIONAL BLOCK DIAGRAM

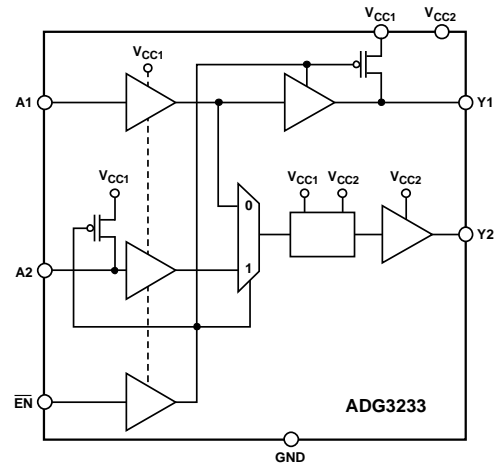


Figure 1.

## GENERAL DESCRIPTION

The [ADG3233](#)<sup>1</sup> is a bypass switch designed on a submicron process that operates from supplies as low as 1.65 V. The device is guaranteed for operation over the supply range 1.65 V to 3.6 V. It operates from two supply voltages, allowing bidirectional level translation, that is, it translates low voltages to higher voltages and vice versa. The signal path is unidirectional, meaning data may only flow from A → Y.

This type of device may be used in applications that require a bypassing function. It is ideally suited to bypassing devices in a JTAG chain or in a daisy-chain loop. One switch could be used for each device or a number of devices, thus allowing easy bypassing of one or more devices in a chain. This may be particularly useful in reducing the time overhead in testing devices in the JTAG chain or in daisy-chain applications where the user does not wish to change the settings of a particular device.

The bypass switch is packaged in two of the smallest footprints available for its required pin count. The 8-lead SOT-23 package requires only 2.9 mm × 2.8 mm board space, while the MSOP package occupies approximately 3 mm × 4.9 mm board area.

## PRODUCT HIGHLIGHTS

1. Bidirectional level translation matches any voltage level from 1.65 V to 3.6 V.
2. The bypass switch offers high performance and is fully guaranteed across the supply range.
3. Short circuit protection.
4. Tiny 8-lead SOT-23 package and 8-lead MSOP.

Table 1. Truth Table

EN	Signal Path	Function
L	A1 → Y2, Y1 → V <sub>CC1</sub>	Enable bypass mode
H	A1 → Y1, A2 → Y2	Enable normal mode

<sup>1</sup> U.S. Patent Number: 7,369,385 B2.

### Rev. C

### Document Feedback

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

**TABLE OF CONTENTS**

Features .....	1	ESD Caution.....	6
Applications.....	1	Pin Configuration and Function Descriptions.....	7
Functional Block Diagram .....	1	Typical Performance Characteristics .....	8
General Description .....	1	Theory of Operation .....	13
Product Highlights .....	1	A1 and $\overline{\text{EN}}$ Input .....	13
Revision History .....	2	Normal Operation.....	13
Specifications.....	3	Bypass Operation .....	14
Test Waveforms.....	5	Outline Dimensions .....	15
Absolute Maximum Ratings.....	6	Ordering Guide .....	16

**REVISION HISTORY**

**4/15—Rev. B to Rev. C**

Changes to Table 4.....	7
Changes to Ordering Guide .....	16

**7/13—Rev. A to Rev. B**

Changes to Table 1.....	1
-------------------------	---

**7/11—Rev. 0 to Rev. A**

Changes to Patent Number, General Description Section, and Product Highlights Section .....	1
Changes to $V_{CC} = V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 0.2 \text{ V}$ , ENABLE Time $\overline{\text{EN}} \rightarrow \text{Y1}$ , Table 2 .....	4
Changes to Table 3.....	6
Updated Outline Dimensions .....	15
Changes to Ordering Guide .....	16

**5/03—Revision 0: Initial Version**

## SPECIFICATIONS

$V_{CC1} = V_{CC2} = 1.65\text{ V to }3.6\text{ V}$ ,  $GND = 0\text{ V}$ , all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 2.

Parameter <sup>1</sup>	Symbol	Test Conditions/Comments	Min	Typ <sup>2</sup>	Max	Unit
LOGIC INPUTS/OUTPUTS <sup>3</sup>						
Input High Voltage <sup>4</sup>	$V_{IH}$	$V_{CC2} = 1.65\text{ V to }3.6\text{ V}$ , $GND = 0\text{ V}$ $V_{CC1} = 3.0\text{ V to }3.6\text{ V}$ $V_{CC1} = 2.3\text{ V to }2.7\text{ V}$ $V_{CC1} = 1.65\text{ V to }1.95\text{ V}$	1.35 1.35 $0.65 \times V_{CC}$			V V V
Input Low Voltage <sup>4</sup>	$V_{IL}$	$V_{CC1} = 3.0\text{ V to }3.6\text{ V}$ $V_{CC1} = 2.3\text{ V to }2.7\text{ V}$ $V_{CC1} = 1.65\text{ V to }1.95\text{ V}$			0.8 0.7 $0.35 \times V_{CC}$	V V V
Output High Voltage (Y1)	$V_{OH}$	$I_{OH} = -100\ \mu\text{A}$ , $V_{CC1} = 3.0\text{ V to }3.6\text{ V}$ $I_{OH} = -100\ \mu\text{A}$ , $V_{CC1} = 2.3\text{ V to }2.7\text{ V}$ $I_{OH} = -100\ \mu\text{A}$ , $V_{CC1} = 1.65\text{ V to }1.95\text{ V}$ $I_{OH} = -4\text{ mA}$ , $V_{CC1} = 2.3\text{ V to }2.7\text{ V}$ $I_{OH} = -4\text{ mA}$ , $V_{CC1} = 1.65\text{ V to }1.95\text{ V}$	2.4 2.0 $V_{CC} - 0.45$ 2.0 $V_{CC} - 0.45$			V V V V V
Output Low Voltage (Y1)	$V_{OL}$	$I_{OH} = -8\text{ mA}$ , $V_{CC1} = 3.0\text{ V to }3.6\text{ V}$ $I_{OL} = 100\ \mu\text{A}$ , $V_{CC1} = 3.0\text{ V to }3.6\text{ V}$ $I_{OL} = 100\ \mu\text{A}$ , $V_{CC1} = 2.3\text{ V to }2.7\text{ V}$ $I_{OL} = 100\ \mu\text{A}$ , $V_{CC1} = 1.65\text{ V to }1.95\text{ V}$ $I_{OL} = 4\text{ mA}$ , $V_{CC1} = 2.3\text{ V to }2.7\text{ V}$ $I_{OL} = 4\text{ mA}$ , $V_{CC1} = 1.65\text{ V to }1.95\text{ V}$ $I_{OL} = 8\text{ mA}$ , $V_{CC1} = 3.0\text{ V to }3.6\text{ V}$	2.4		0.40 0.40 0.45 0.40 0.45 0.40	V V V V V V V
LOGIC OUTPUTS <sup>3</sup>						
Output High Voltage (Y2)	$V_{OH}$	$V_{CC1} = 1.65\text{ V to }3.6\text{ V}$ , $GND = 0\text{ V}$ $I_{OH} = -100\ \mu\text{A}$ , $V_{CC2} = 3.0\text{ V to }3.6\text{ V}$ $I_{OH} = -100\ \mu\text{A}$ , $V_{CC2} = 2.3\text{ V to }2.7\text{ V}$ $I_{OH} = -100\ \mu\text{A}$ , $V_{CC2} = 1.65\text{ V to }1.95\text{ V}$ $I_{OH} = -4\text{ mA}$ , $V_{CC2} = 2.3\text{ V to }2.7\text{ V}$ $I_{OH} = -4\text{ mA}$ , $V_{CC2} = 1.65\text{ V to }1.95\text{ V}$ $I_{OH} = -8\text{ mA}$ , $V_{CC2} = 3.0\text{ V to }3.6\text{ V}$	2.4 2.0 $V_{CC} - 0.45$ 2.0 $V_{CC} - 0.45$ 2.4			V V V V V V
Output Low Voltage (Y2)	$V_{OL}$	$I_{OL} = 100\ \mu\text{A}$ , $V_{CC2} = 3.0\text{ V to }3.6\text{ V}$ $I_{OL} = 100\ \mu\text{A}$ , $V_{CC2} = 2.3\text{ V to }2.7\text{ V}$ $I_{OL} = 100\ \mu\text{A}$ , $V_{CC2} = 1.65\text{ V to }1.95\text{ V}$ $I_{OL} = 4\text{ mA}$ , $V_{CC2} = 2.3\text{ V to }2.7\text{ V}$ $I_{OL} = 4\text{ mA}$ , $V_{CC2} = 1.65\text{ V to }1.95\text{ V}$ $I_{OL} = 8\text{ mA}$ , $V_{CC2} = 3.0\text{ V to }3.6\text{ V}$			0.40 0.40 0.45 0.40 0.45 0.40	V V V V V V
SWITCHING CHARACTERISTICS <sup>4,5</sup>						
$V_{CC} = V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 0.3\text{ V}$ Propagation Delay, $t_{PD}$						
A1 → Y1 Normal Mode	$t_{PHL}$ , $t_{PLH}$	$C_L = 30\text{ pF}$ , $V_T = V_{CC}/2$		3.5	5.4	ns
A2 → Y2 Normal Mode	$t_{PHL}$ , $t_{PLH}$	$C_L = 30\text{ pF}$ , $V_T = V_{CC}/2$		3.5	5.4	ns
A1 → Y2 Bypass Mode	$t_{PHL}$ , $t_{PLH}$	$C_L = 30\text{ pF}$ , $V_T = V_{CC}/2$		4	6.5	ns
ENABLE Time $\overline{EN} \rightarrow Y1$	$t_{EN}^-$	$C_L = 30\text{ pF}$ , $V_T = V_{CC}/2$		4	6	ns
DISABLE Time $\overline{EN} \rightarrow Y1$	$t_{DIS}$	$C_L = 30\text{ pF}$ , $V_T = V_{CC}/2$		2.8	4	ns
ENABLE Time $\overline{EN} \rightarrow Y2$	$t_{EN}^-$	$C_L = 30\text{ pF}$ , $V_T = V_{CC}/2$		4.5	6.5	ns
DISABLE Time $\overline{EN} \rightarrow Y2$	$t_{DIS}$	$C_L = 30\text{ pF}$ , $V_T = V_{CC}/2$		4	6.5	ns

Parameter <sup>1</sup>	Symbol	Test Conditions/Comments	Min	Typ <sup>2</sup>	Max	Unit
$V_{CC} = V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 0.2\text{ V}$						
Propagation Delay, $t_{PD}$						
A1 → Y1 Normal Mode	$t_{PHL}, t_{PLH}$	$C_L = 30\text{ pF}, V_T = V_{CC}/2$		4.5	6.2	ns
A2 → Y2 Normal Mode	$t_{PHL}, t_{PLH}$	$C_L = 30\text{ pF}, V_T = V_{CC}/2$		4.5	6.2	ns
A1 → Y2 Bypass Mode	$t_{PHL}, t_{PLH}$	$C_L = 30\text{ pF}, V_T = V_{CC}/2$		4.5	6.5	ns
ENABLE Time $\overline{EN} \rightarrow Y1$	$t_{EN}^-$	$C_L = 30\text{ pF}, V_T = V_{CC}/2$		5	7.2	ns
DISABLE Time $\overline{EN} \rightarrow Y1$	$t_{DIS}$	$C_L = 30\text{ pF}, V_T = V_{CC}/2$		3.2	4.7	ns
ENABLE Time $\overline{EN} \rightarrow Y2$	$t_{EN}^-$	$C_L = 30\text{ pF}, V_T = V_{CC}/2$		5	7.7	ns
DISABLE Time $\overline{EN} \rightarrow Y2$	$t_{DIS}$	$C_L = 30\text{ pF}, V_T = V_{CC}/2$		4.8	7.2	ns
$V_{CC} = V_{CC1} = V_{CC2} = 1.8\text{ V} \pm 0.15\text{ V}$						
Propagation Delay, $t_{PD}$						
A1 → Y1 Normal Mode	$t_{PHL}, t_{PLH}$	$C_L = 30\text{ pF}, V_T = V_{CC}/2$		6.7	10	ns
A2 → Y2 Normal Mode	$t_{PHL}, t_{PLH}$	$C_L = 30\text{ pF}, V_T = V_{CC}/2$		6.5	10	ns
A1 → Y2 Bypass Mode	$t_{PHL}, t_{PLH}$	$C_L = 30\text{ pF}, V_T = V_{CC}/2$		6.5	10.25	ns
ENABLE Time $\overline{EN} \rightarrow Y1$	$t_{EN}^-$	$C_L = 30\text{ pF}, V_T = V_{CC}/2$		7	10.5	ns
DISABLE Time $\overline{EN} \rightarrow Y1$	$t_{DIS}$	$C_L = 30\text{ pF}, V_T = V_{CC}/2$		4.4	6.5	ns
ENABLE Time $\overline{EN} \rightarrow Y2$	$t_{EN}^-$	$C_L = 30\text{ pF}, V_T = V_{CC}/2$		7	12	ns
DISABLE Time $\overline{EN} \rightarrow Y2$	$t_{DIS}$	$C_L = 30\text{ pF}, V_T = V_{CC}/2$		6.5	10.5	ns
Input Leakage Current	$I_I$	$0 \leq V_{IN} \leq 3.6\text{ V}$			±1	μA
Output Leakage Current	$I_O$	$0 \leq V_{IN} \leq 3.6\text{ V}$			±1	μA
<b>POWER REQUIREMENTS</b>						
Power Supply Voltages	$V_{CC1}$		1.65		3.6	V
	$V_{CC2}$		1.65		3.6	V
Quiescent Power Supply Current	$I_{CC1}$	Digital inputs = 0 V or $V_{CC}$			2	μA
	$I_{CC2}$	Digital inputs = 0 V or $V_{CC}$			2	μA
Increase in $I_{CC}$ per Input	$\Delta I_{CC1}$	$V_{CC} = 3.6\text{ V}$ , one input at 3.0 V; others at $V_{CC}$ or GND			0.75	μA

<sup>1</sup> Temperature range is as follows: B Version:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

<sup>2</sup> All typical values are at  $V_{CC} = V_{CC1} = V_{CC2}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise stated.

<sup>3</sup>  $V_{IL}$  and  $V_{IH}$  levels are specified with respect to  $V_{CC1}$ ,  $V_{OH}$ , and  $V_{OL}$  levels for Y1 are specified with respect to  $V_{CC1}$ , and  $V_{OH}$ , and  $V_{OL}$  levels are specified for Y2 with respect to  $V_{CC2}$ .

<sup>4</sup> Guaranteed by design, not subject to production test.

<sup>5</sup> See the Test Waveforms section.

TEST WAVEFORMS

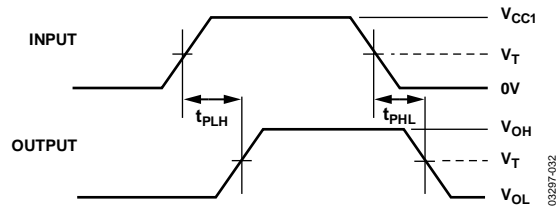


Figure 2. Propagation Delay

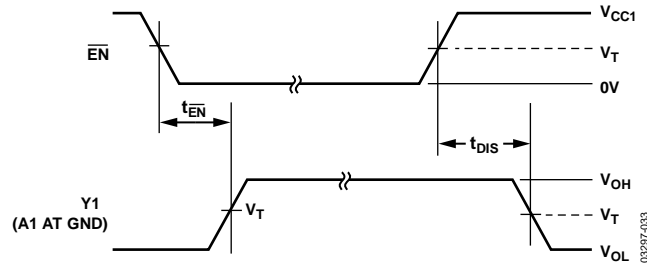


Figure 3. Y1 Enable and Disable Times

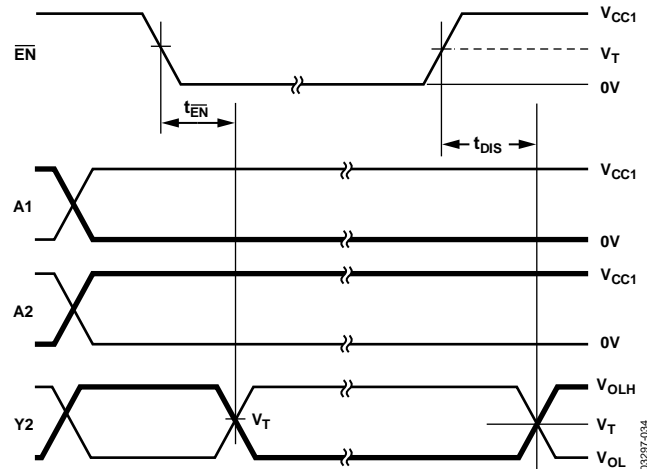


Figure 4. Y2 Enable and Disable Times

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Rating
$V_{CC}$ to GND	-0.3 V to +4.6 V
Digital Inputs to GND	-0.3 V to +4.6 V
A1, $\overline{\text{EN}}$	-0.3 V to +4.6 V
A2	-0.3 V to $V_{CC1} + 0.3$ V
DC Output Current	25 mA
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
8-Lead MSOP	
$\theta_{JA}$ Thermal Impedance	206°C/W
$\theta_{JC}$ Thermal Impedance	43°C/W
8-Lead SOT-23	
$\theta_{JA}$ Thermal Impedance	211°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C
Soldering (Pb-Free)	
Reflow, Peak Temperature	260(+0/-5)°C
Time at Peak Temperature	20 sec to 40 sec

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating may be applied at any one time.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

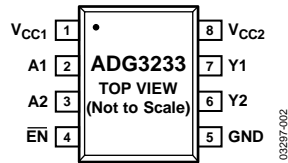


Figure 5. 8-Lead SOT-23 Package (RJ-8)



Figure 6. 8-Lead MSOP Package (RM-8)

Table 4. Pin Function Descriptions

Pin No.		Mnemonic	Description
RJ-8	RM-8		
1	8	$V_{CC1}$	Supply Voltage 1, can be any supply voltage from 1.65 V to 3.6 V.
8	1	$V_{CC2}$	Supply Voltage 2, can be any supply voltage from 1.65 V to 3.6 V.
2	7	A1	Input Referred to $V_{CC1}$ .
3	6	A2	Input Referred to $V_{CC1}$ .
7	2	Y1	Output Referred to $V_{CC1}$ .
6	3	Y2	Output Referred to $V_{CC2}$ . Voltage levels appearing at Y2 will be translated from a $V_{CC1}$ voltage level to a $V_{CC2}$ voltage level.
4	5	$\overline{EN}$	Active Low Device Enable. When low, bypass mode is enabled; when high, the device is in normal mode.
5	4	GND	Device Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

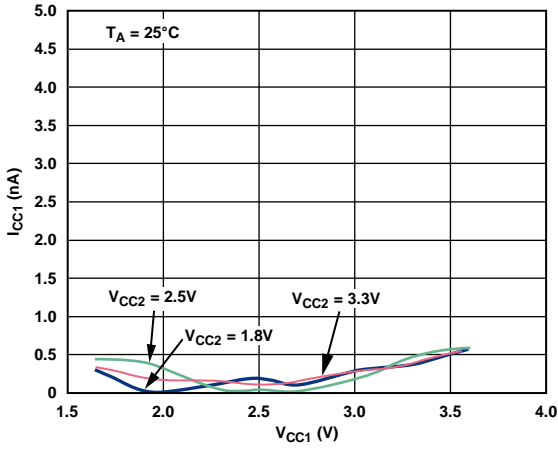


Figure 7.  $I_{CC1}$  vs.  $V_{CC1}$

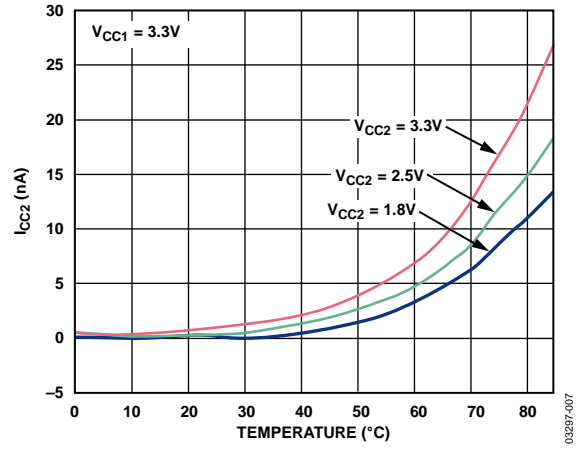


Figure 10.  $I_{CC2}$  vs. Temperature

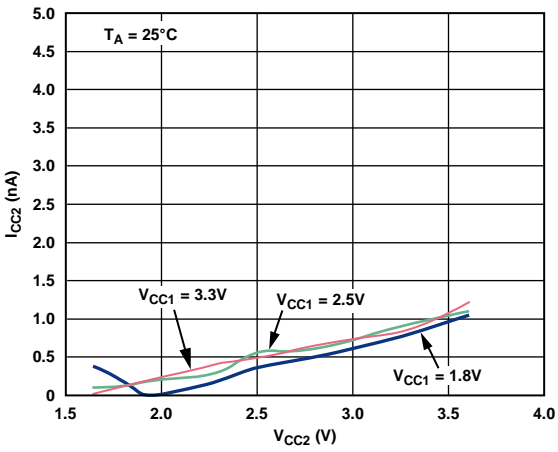


Figure 8.  $I_{CC2}$  vs.  $V_{CC2}$

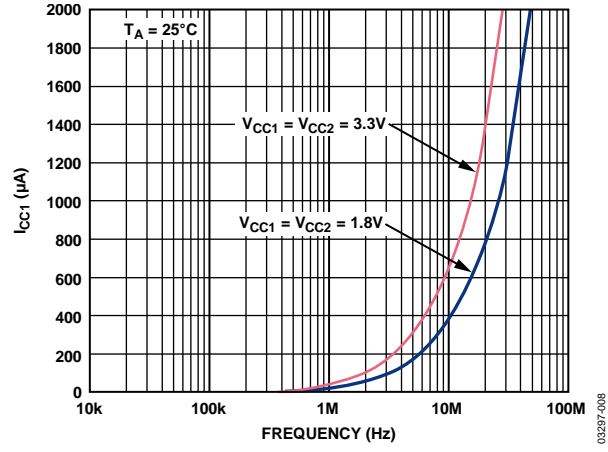


Figure 11.  $I_{CC1}$  vs. Frequency, Normal Mode

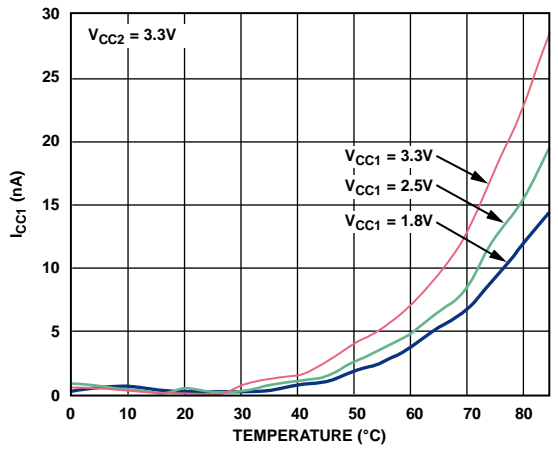


Figure 9.  $I_{CC1}$  vs. Temperature

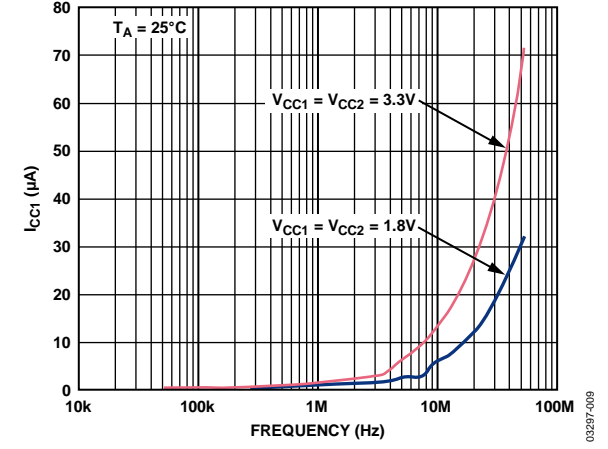


Figure 12.  $I_{CC1}$  vs. Frequency, Bypass Mode



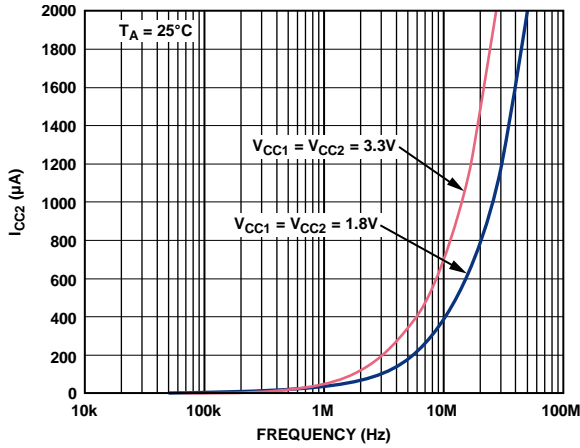


Figure 13.  $I_{CC2}$  vs. Frequency, Normal Mode

03297-010

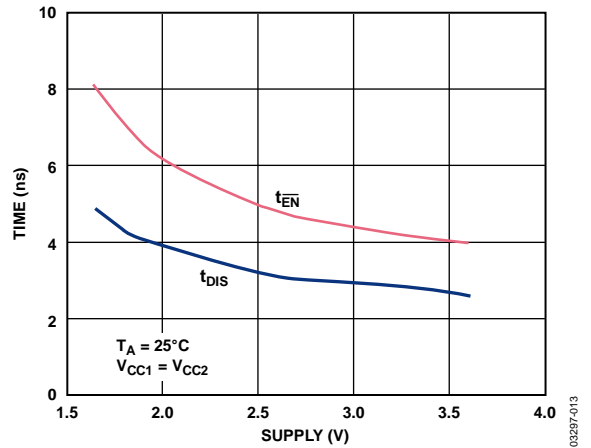


Figure 16. Y2 Enable, Disable Time vs. Supply

03297-013

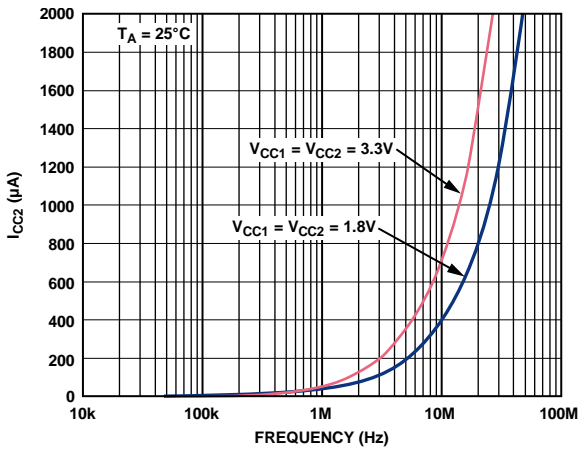


Figure 14.  $I_{CC2}$  vs. Frequency, Bypass Mode

03297-011

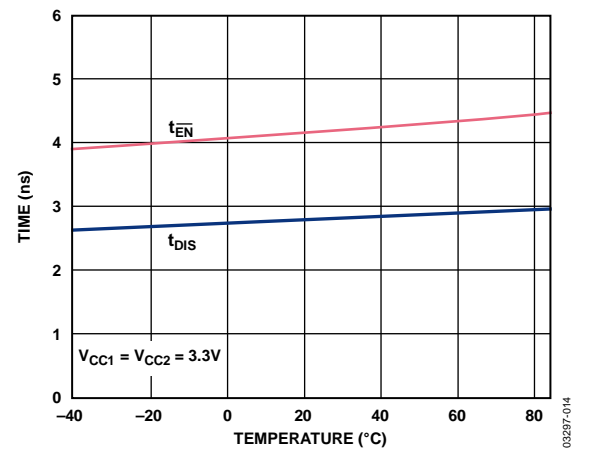


Figure 17. Y1 Enable, Disable Time vs. Temperature

03297-014

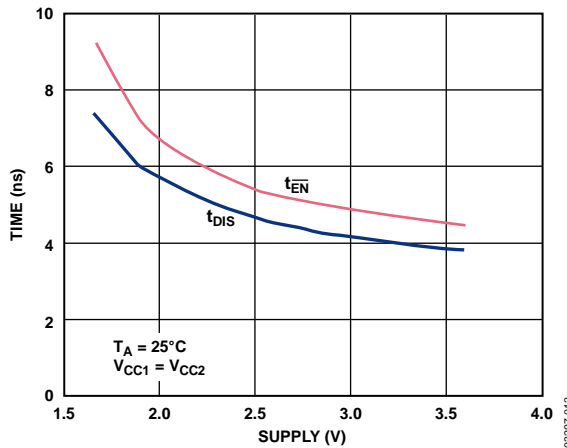


Figure 15. Y1 Enable, Disable Time vs. Supply

03297-012

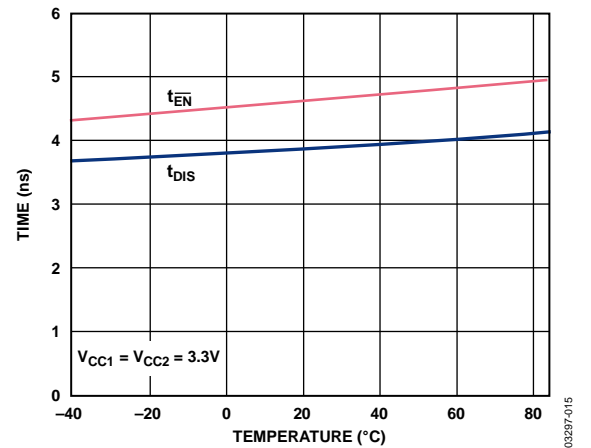


Figure 18. Y2 Enable, Disable Time vs. Temperature

03297-015

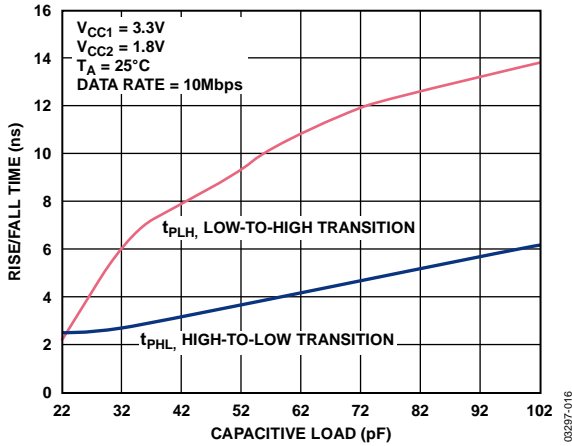


Figure 19. Rise/Fall Time vs. Capacitive Load, A1 → Y1, A2 → Y2

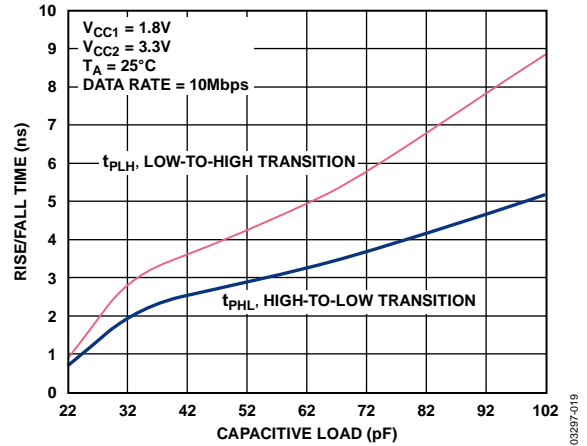


Figure 22. Rise/Fall Time vs. Capacitive Load, A1 → Y2, Bypass Mode

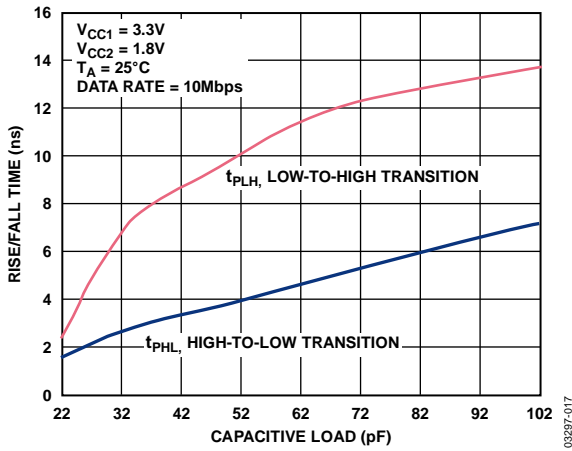


Figure 20. Rise/Fall Time vs. Capacitive Load, A1 → Y2, Bypass Mode

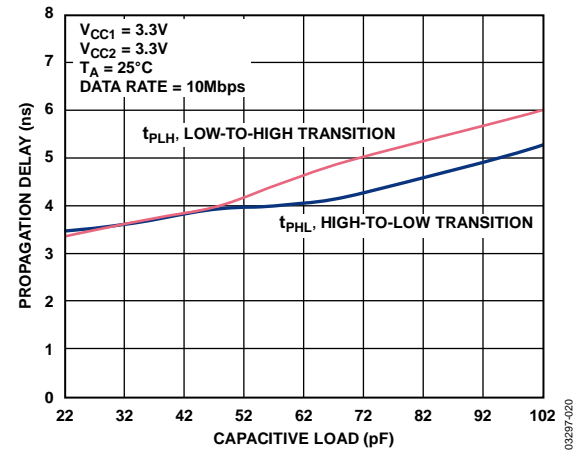


Figure 23. Propagation Delay vs. Capacitive Load A1 → Y1

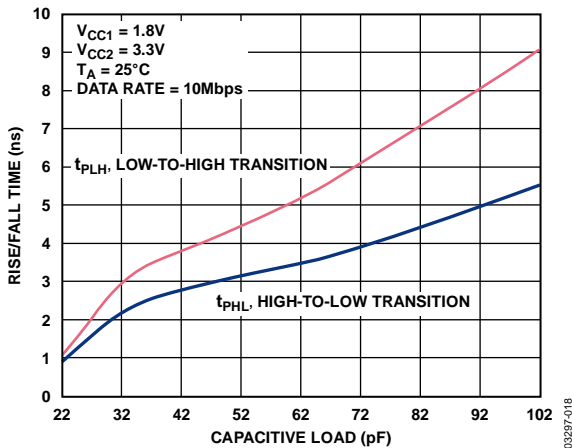


Figure 21. Rise/Fall Time vs. Capacitive Load, A1 → Y1, A2 → Y2

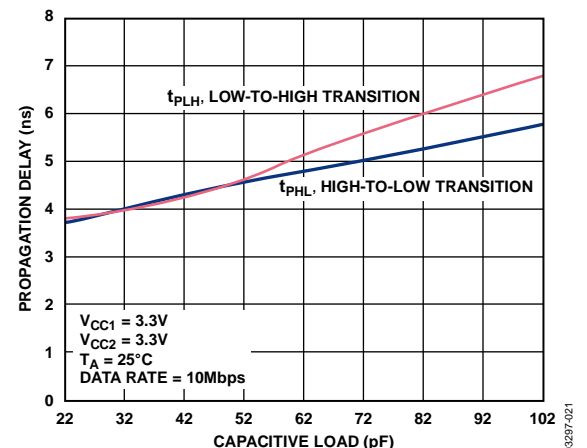


Figure 24. Propagation Delay vs. Capacitive Load A2 → Y2

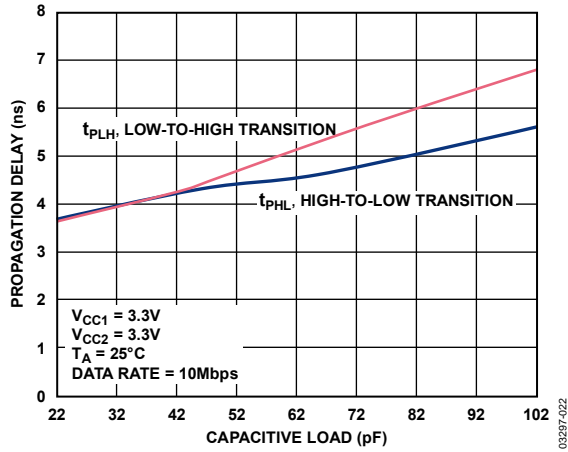


Figure 25. Propagation Delay vs. Capacitive Load A1 → Y2, Bypass Mode

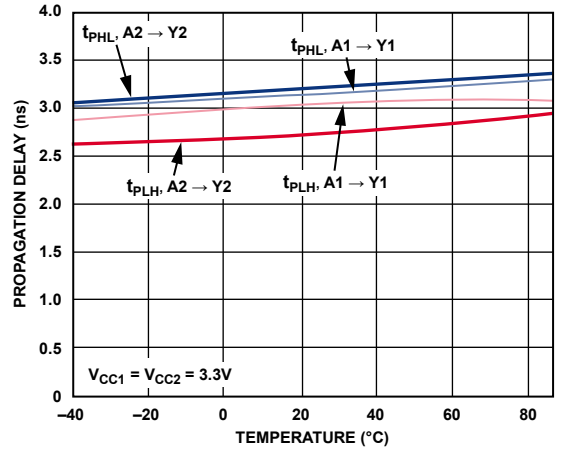


Figure 28. Propagation Delay vs. Temperature, Normal Mode

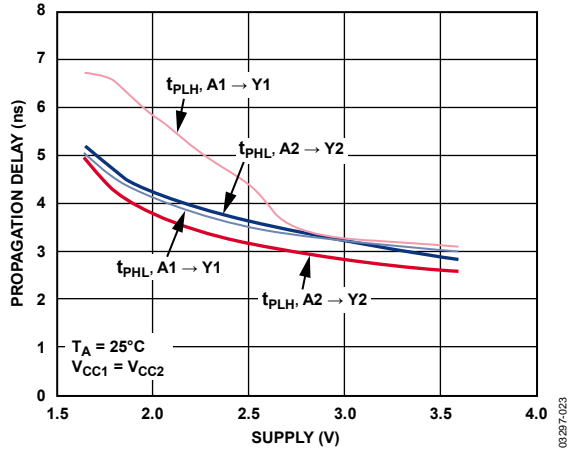


Figure 26. Propagation Delay vs. Supply, Normal Mode

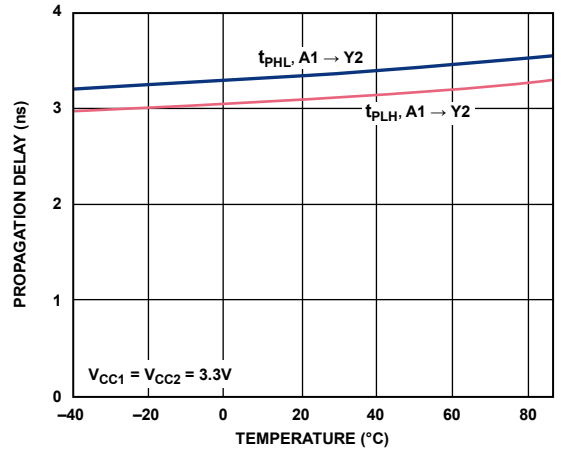


Figure 29. Propagation Delay vs. Temperature, Bypass Mode

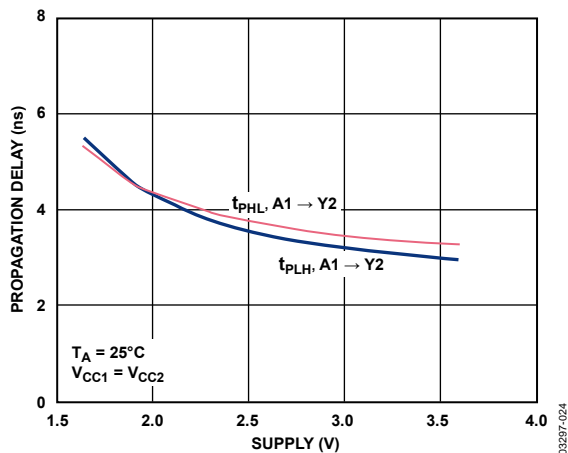


Figure 27. Propagation Delay vs. Supply, Bypass Mode

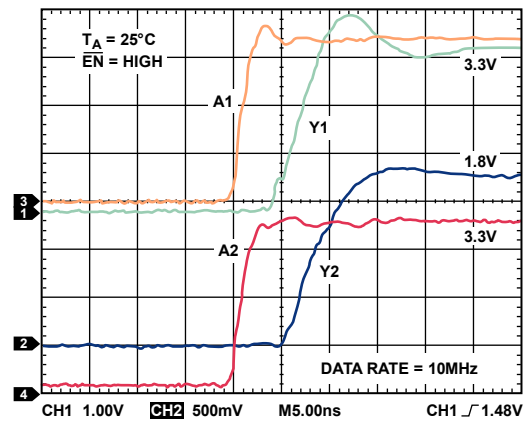


Figure 30. Normal Mode  $V_{CC1} = 3.3V$ ,  $V_{CC2} = 1.8V$

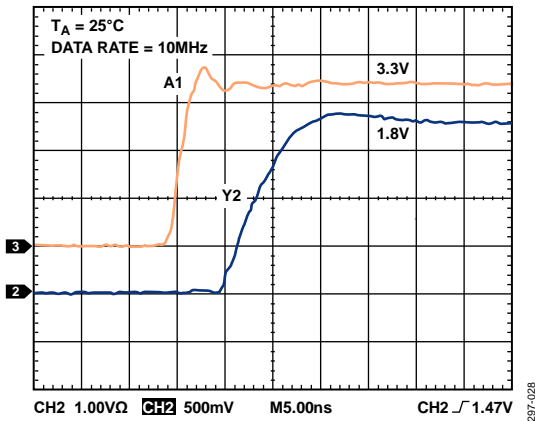


Figure 31. Bypass Mode,  $V_{CC1} = 3.3V$ ,  $V_{CC2} = 1.8V$

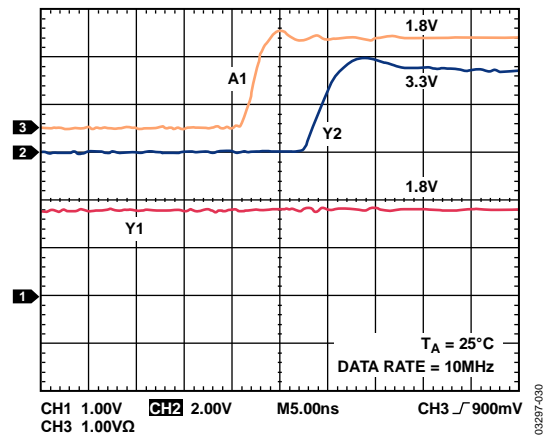


Figure 33. Bypass Mode,  $V_{CC1} = 1.8V$ ,  $V_{CC2} = 3.3V$

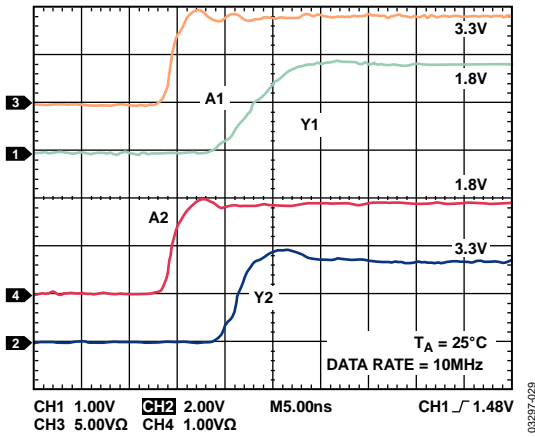


Figure 32. Normal Mode,  $V_{CC1} = 1.8V$ ,  $V_{CC2} = 3.3V$

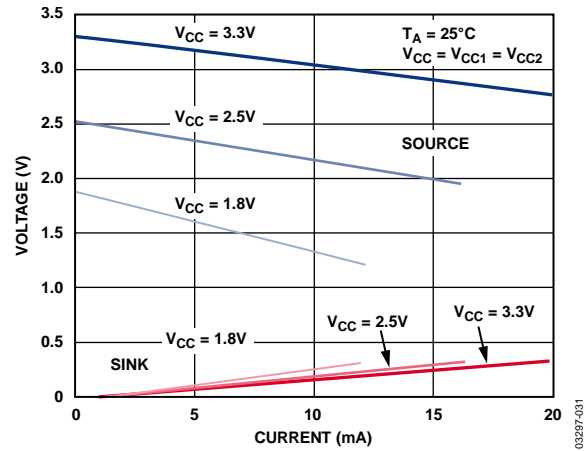


Figure 34. Y1 and Y2 Source and Sink Current

## THEORY OF OPERATION

The ADG3233 is a bypass switch designed on a submicron process that operates from supplies as low as 1.65 V. The device is guaranteed for operation over the supply range 1.65 V to 3.6 V. It operates from two supply voltages, allowing bidirectional level translation, that is, it translates low voltages to higher voltages and vice versa. The signal path is unidirectional, meaning data may only flow from A → Y.

### A1 AND $\overline{\text{EN}}$ INPUT

The A1 and enable ( $\overline{\text{EN}}$ ) inputs have  $V_{\text{IL}}/V_{\text{IH}}$  logic levels so that the part can accept logic levels of  $V_{\text{OL}}/V_{\text{OH}}$  from Device 0 or the controlling device independent of the value of the supply being used by the controlling device. These inputs (A1,  $\overline{\text{EN}}$ ) are capable of accepting inputs outside the  $V_{\text{CC1}}$  supply range. For example, the  $V_{\text{CC1}}$  supply applied to the bypass switch could be 1.8 V while Device 0 could be operating from a 2.5 V or 3.3 V supply rail, there are no internal diodes to the supply rails, so the device can handle inputs above the supply but inside the absolute maximum ratings.

### NORMAL OPERATION

Figure 35 shows the bypass switch being used in normal mode. In this mode, the signal paths are from A1 → Y1 and A2 → Y2. The device will level translate the signal applied to A1 to a  $V_{\text{CC1}}$  logic level (this level translation can be either to a higher or lower supply) and route the signal to the Y1 output, which will have standard  $V_{\text{OL}}/V_{\text{OH}}$  levels for  $V_{\text{CC1}}$  supplies. The signal is then passed through Device 1 and back to the A2 input pin of the bypass switch.

The logic level inputs of A2 are with respect to the  $V_{\text{CC1}}$  supply. The signal will be level translated from  $V_{\text{CC1}}$  to  $V_{\text{CC2}}$  and routed to the Y2 output pin of the bypass switch. Y2 output logic levels are with respect to the  $V_{\text{CC2}}$  supply.

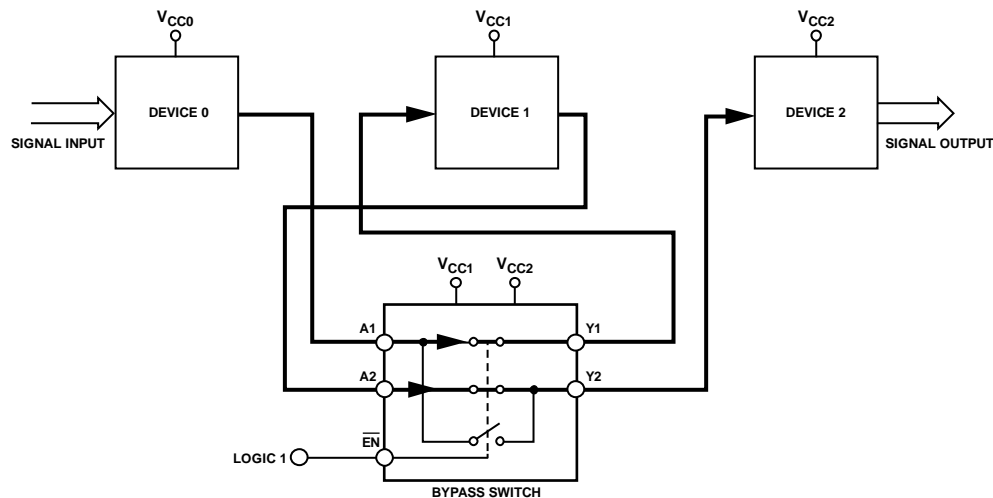


Figure 35. Bypass Switch in Normal Mode

03237-035

**BYPASS OPERATION**

Figure 36 illustrates the device as used in bypass mode. The signal path is now from A1 directly to Y2, thus bypassing Device 1 completely. The signal will be level translated to a  $V_{CC2}$  logic level and available on Y2, where it may be applied directly to the input of Device 2. In bypass mode, Y1 is pulled up to  $V_{CC1}$ .

The three supplies in Figure 35 and Figure 36 may be any combination of supplies, that is.,  $V_{CC0}$ ,  $V_{CC1}$ , and  $V_{CC2}$  may be any combination of supplies, for example, 1.8 V, 2.5 V, and 3.3 V.

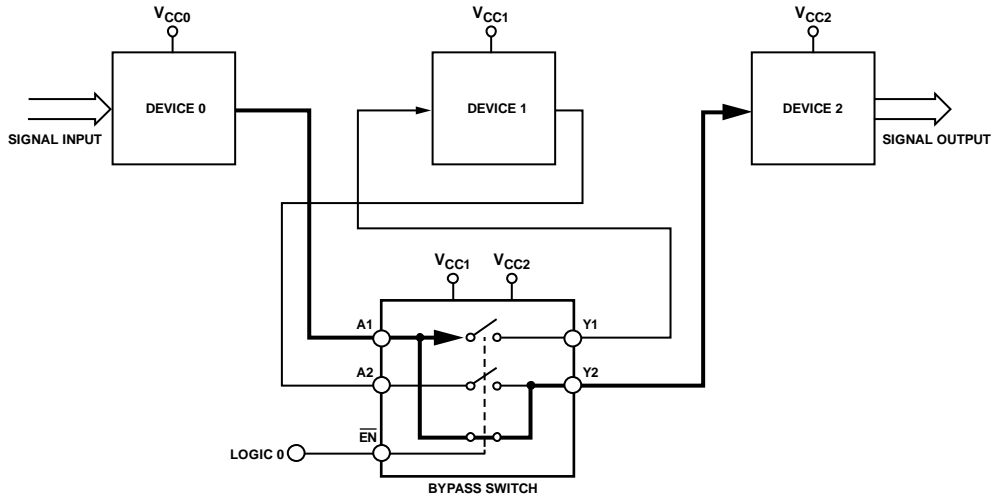
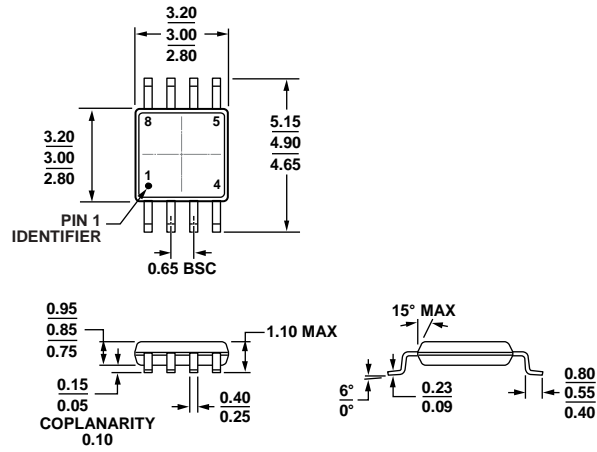


Figure 36. Bypass Switch in Bypass Mode

03237-036

# OUTLINE DIMENSIONS

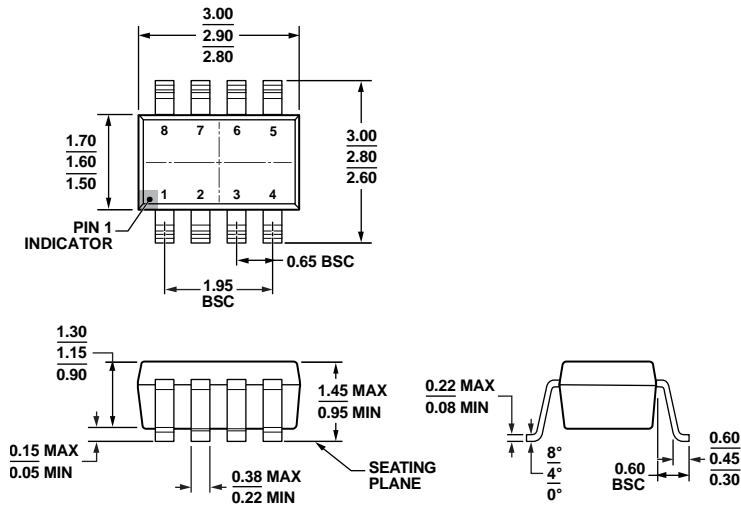


COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 37. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

10-07-2008-B



COMPLIANT TO JEDEC STANDARDS MO-178-BA

Figure 38. 8-Lead Small Outline Transistor Package [SOT-23] (RJ-8)

Dimensions shown in millimeters

12-16-2008-A

**ORDERING GUIDE**

<b>Model<sup>1</sup></b>	<b>Temperature Range</b>	<b>Package Description</b>	<b>Branding</b>	<b>Package Option</b>
ADG3233BRJ-REEL7	-40°C to +85°C	8-Lead SOT-23	W1B	RJ-8
ADG3233BRJZ-REEL7	-40°C to +85°C	8-Lead SOT-23	S1S	RJ-8
ADG3233BRMZ	-40°C to +85°C	8-Lead MSOP	S1S	RM-8

<sup>1</sup> Z = RoHS Compliant Part.



# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Analog Devices Inc.:](#)

[ADG3233BRJZ-REEL7](#) [ADG3233BRMZ](#)