

TD6710AN/AF

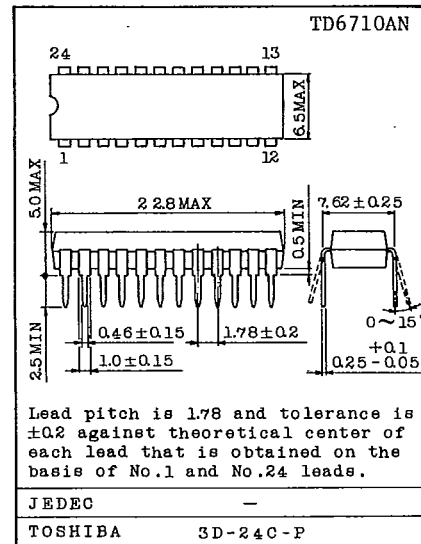
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14-BITS LOW POWER D/A CONVERTER

TD6710AN/AF is dual-slope single-integral 14-bits low-power D/A converter, designed for use in PCM digital audio equipments.

- Corresponding with 2's complement code.
- Reduced number of external components by means of built-in sample hold circuit.
- Corresponding with sampling frequency 44.1kHz.
- Alternate D/A conversion of both signals of right and left stereo channels.
- +5V single power supply.
- Low power dissipation. ($P_D=100\text{mW TYP.}$)
- S/N ratio : 83.5dB TYP.
- THD : 0.008% TYP.
(Without aperture compensation)

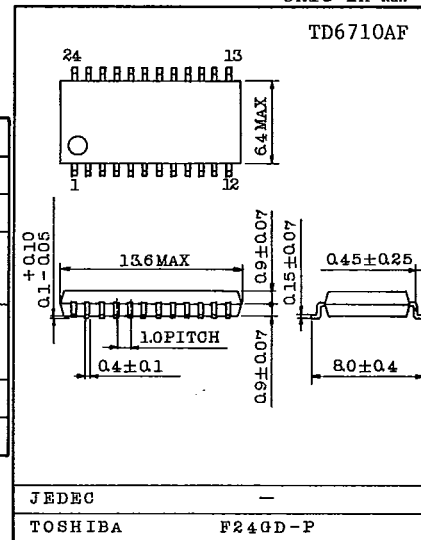
Unit in mm



MAXIMUM RATINGS ($T_a=25^\circ\text{C}$)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Analog Supply Voltage		V_{CCA}	-0.3~8	V
Digital Supply Voltage		V_{CCD}	-0.3~8	V
Input Voltage		V_{IN}	$GND_D-0.3$ $\sim V_{CCD}+0.3$	V
Power Dissipation	TD6710AN	P_D	1300	mW
	TD6710AF		400	
Operating Temperature		T_{opr}	-25~75	$^\circ\text{C}$
Storage Temperature		T_{stg}	-55~150	$^\circ\text{C}$

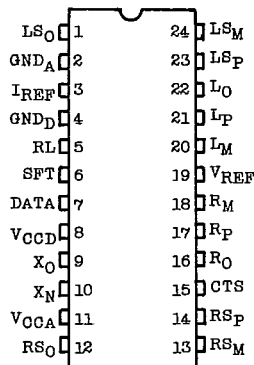
Unit in mm



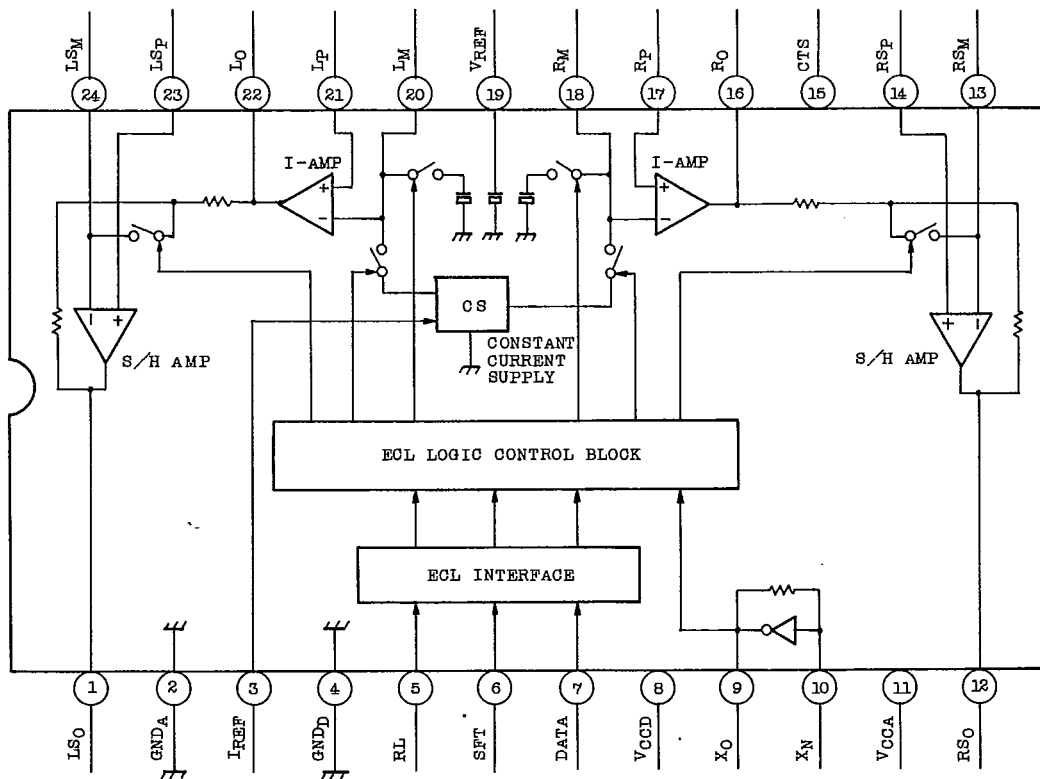
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PIN CONNECTIONS



BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{CCA}=V_{CCD}=5\text{V}$)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V_{CCA}	-		4.5	5	8	V
	V_{CCD}	-		4.5	5	8	
Operating Supply Current	I_{CCA}	1	At non-signal	7.0	10.0	13.0	mA
	I_{CCD}	1		6.4	8.5	10.6	
Input Voltage	"H" Level	V_{IH}	RL, SFT, DATA terminal	2.9	-	-	V
	"L" Level	V_{IL}	"	-	-	1.4	
Input Current	"H" Level	I_{IH}	" $V_{IH}=5\text{V}$	-	-	4	μA
	"L" Level	I_{IL}	" $V_{IL}=0\text{V}$	-	-	1	
Total Harmonic Distortion	THD	1	0dB (full-scale) input	-	-82	-80	dB
SN Ratio	S/N	1	Value of -20dB input, added by +20dB	82	83.5	-	dB
Cross-Talk	C.T	1	Single channel 0dB (full-scale) input	81	83	-	dB
Output Voltage	V_{RSO}	1	0dB (full-scale) input	-3	-2	-	dBV
	V_{LSO}						
Output Differential Voltage	V_{OD}	-	0dB (full-scale) input $V_{RSO}-V_{LSO}$	-0.6	0	0.6	dBV
Built-in Reference Voltage	V_{REF}	-		2.2	2.3	2.4	V
S/H AMP Reference Voltage	V_{RSP}	-		2.4	2.5	2.6	V
	V_{LSP}						
Operation Frequency	f_{op}	-		16.5	16.9	20	MHz

TEST CIRCUIT 1 : Application circuit is used, and RL, SFT, DATA, analog output are as follows.

- . $f_{RL}=44.1\text{kHz}$
- . $f_{SFT}=1.4112\text{MHz}$
- . DATA : $f=1\text{kHz}$
- . Analog output : -3dBV at 0dB input

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FUNCTION OF EACH PIN

PIN No.	SYMBOL	FUNCTION DESCRIPTION	REMARKS
1	LSO	Lch sample-hold output terminal.	
2	GND _A	Analog GND terminal.	
3	I _{REF}	Reference current input terminal. Input for determining current of constant current supply. Connect the resistor (68k Ω) between this terminal and GND _A .	
4	GND _D	Digital GND terminal.	
5	RL	Input data L,Rch indication signal input terminal. Used as control signal in LSI. Requested to be input in synchronization with SFT trailing edge. $f_{RL}=44.1\text{kHz}$ duty cycle=50%	
6	SFT	Shift clock input terminal. Clock for reading bit-serially PCM digital audio 16-bit data into LSI from MSB side. $f_{SFT}=1.4112\text{MHz}$, duty cycle=50%	
7	DATA	PCM digital audio data input terminal. Requested to be input bit-serially (each 16-bit data) from MSB side in synchronization with SFT trailing edge. Corresponding to RL signal "L" level=Lch, "H" level=Rch.	
8	V _{CCD}	Digital power supply voltage terminal. +5V	
9 10	X _O X _N	Input terminal for oscillation circuit. Modified colpitts oscillation circuit is constructed through the combination of X'tal oscillation terminal with C.	Ceralok is applicable. 16.9MHz can be supplied to X _N from outside. (upto CMOS level). Connect X _O to V _{CCD} .
11	V _{CCA}	Analog power supply voltage terminal. +5V	

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PIN No.	SYMBOL	FUNCTION DESCRIPTION	REMARKS
12	RSO	Rch sample·hold output terminal.	
13	RSM	Negative input terminal for Rch sample·hold ope-amp. Hold capacitor is connected to RSO and RSM.	
14	RSp	Positive input terminal for Rch sample·hold ope-amp.	
15	CST	Internal constant current supply terminal. De-coupling capacitor is connected to ground.	
16	RO	Rch integrator output terminal.	
17	Rp	Positive input terminal for Rch integrator ope-amp.	
18	RM	Negative input terminal for Rch integrator ope-amp. Integrating capacitor is connected to RO and RM.	
19	VREF	Integrator reference power supply voltage terminal. Power supply is constructed inside LSI and is connected to positive inputs Lp,Rp for L, Rch integrator ope-amp.	
20	LM	Negative input terminal for Lch integrator ope-amp. Integrating capacitor is connected to LO and LM.	
21	Lp	Positive input terminal for Lch integrator ope-amp.	
22	LO	Lch integrator output terminal.	
23	LSp	Positive input terminal for Lch sample·hold ope-amp.	
24	LSM	Negative input terminal for Lch sample·hold ope-amp. Hold capacitor is connected to LSO and LSM.	

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DESCRIPTION ON OPERATION OF EACH BLOCK

1. OSCILLATION CIRCUIT

Modified colpitts oscillator can be constructed with internal amplifier by connecting external X'tal (or ceralok) and capacitor.

The oscillation output is input to the control block and is used as the clock pulse for determining the intergration period.

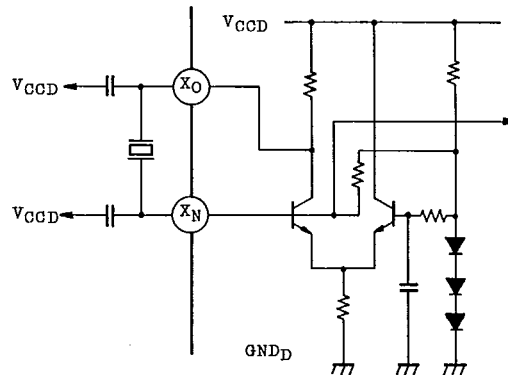


Fig. 1 EXAMPLE FOR APPLICATION OF X'tal CERALOK OSCILLATOR

2. CONTROL BLOCK (ECL LOGIC)

Control block is constructed with the following four blocks as shown in Fig. 2.

- (1) 14-bits shift register : 14-SR
- (2) 7-bits preset type downcounter : M-CNT7 and L-CNT7
- (3) ALL 0 detection circuit : M-ALLO DET and L-ALLO DET
- (4) Timing generator : T.G.

Each signal of RL, SFT and DATA is input to ECL logic interface and DATA is loaded on 14-bits shift register 14SR through the DELAY circuit at SFT leading edge.

The loaded data performs DA conversion of the data, which is set to 14-SR, by means of carrying out the counting and the integrating operations at the same time through using the oscillation output f_{OSC} .

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Finally, this DA converted output is output outside through the samples hold circuit.

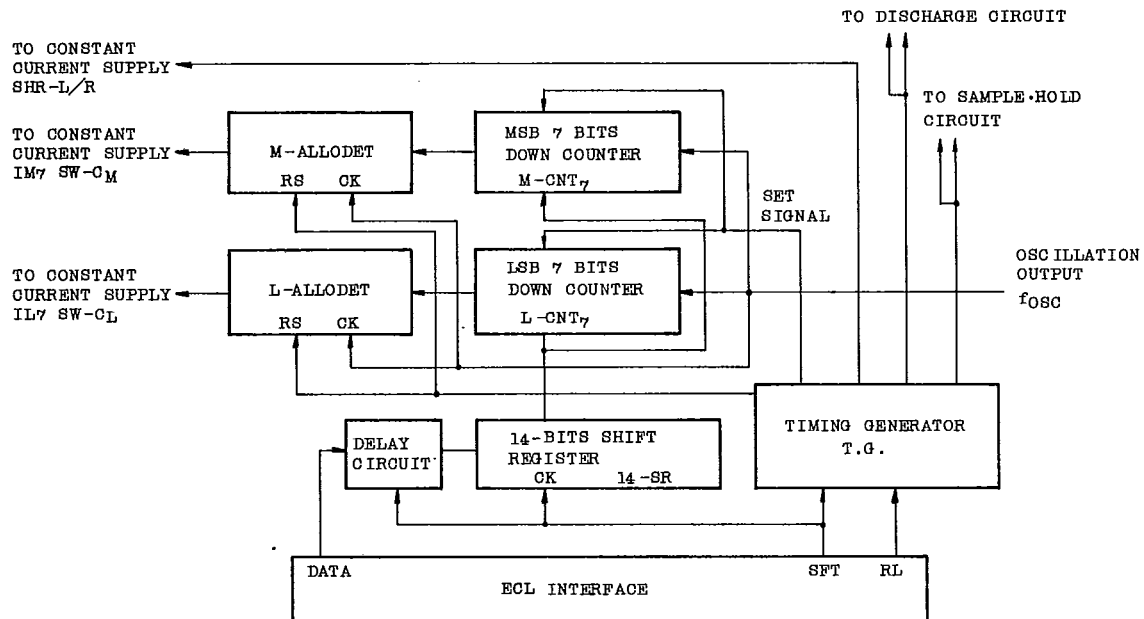


Fig. 2 CONTROL BLOCK CONFIGURATION

Description is made on each block in the following.

(1) 14-bits shift register : 14-SR

Each 16-bits of L and R stereo channel digital audio data is loaded on 14-SR at the leading edge of SFT in order from the most significant bit (MSB) side.

When 16 bits of L or R channel are loaded completely, the 14 bits data are divided into MSB side 7 bits and LSB side 7 bits to be individually set to the down counters M-CNT7 and L-CNT7. (To 14-SR, 14 bits of before the leading and the trailing edges of RL signal.)

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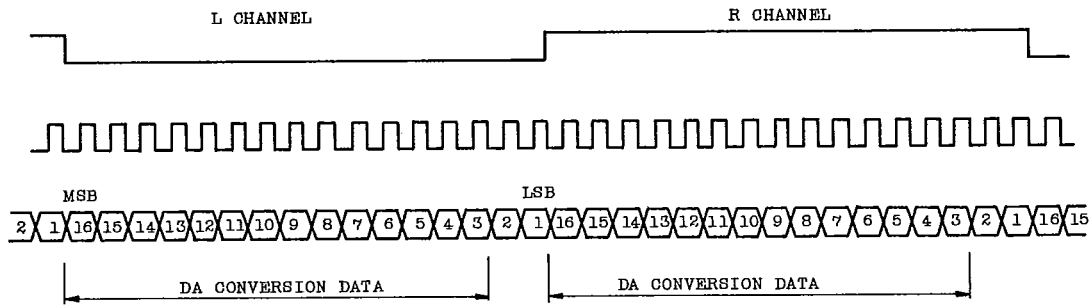


Fig. 3 EACH INPUT SIGNAL TIMING CHART OF RL, SFT AND DATA

(2) Down Counter : M-CNT7, L-CNT7

As soon as the data is set to M-CNT7 and L-CNT7, each counter starts its down-count operation.

Because the input of 14-bits digital audio signal is 2'S complementary code, MSB data D14 of M-CNT7 is inverted and input.

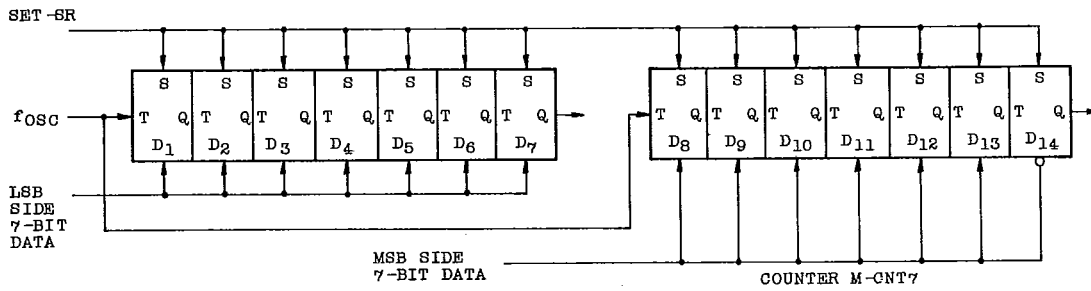


Fig. 4 CONFIGURATION OF COUNTER M-CNT7 AND L-CNT7

(3) ALLO detection circuit of counter : M-ALLO DET, L-ALLO DET

As soon as the data is set to M-CNT7 and L-CNT7, M-ALLO DET and L-ALLO DET are reset by the O-RS signal which is input from T.G. and the constant current supply is connected to the integrating circuit.

The completion of the integrating operation is detected from the state change of the outputs Q14 and Q7 of M-CNT7 and L-CNT7. After M-ALLO DET and L-ALLO DET are set, the constant current supply unit is separated from the integrating circuit.

(4) Timing Generator : T.G.

Through ECL interface circuit, input each signal RL and SFT to output the following signals to each unit.

- . Set signals for M-CNT7 and L-CNT7:
- . Reset signal for ALLO detection circuit:
- . Control signal for sample-hold circuit:
- . Control signal for switching L and R channels of constant current supply:
- . Integrator reset signal:

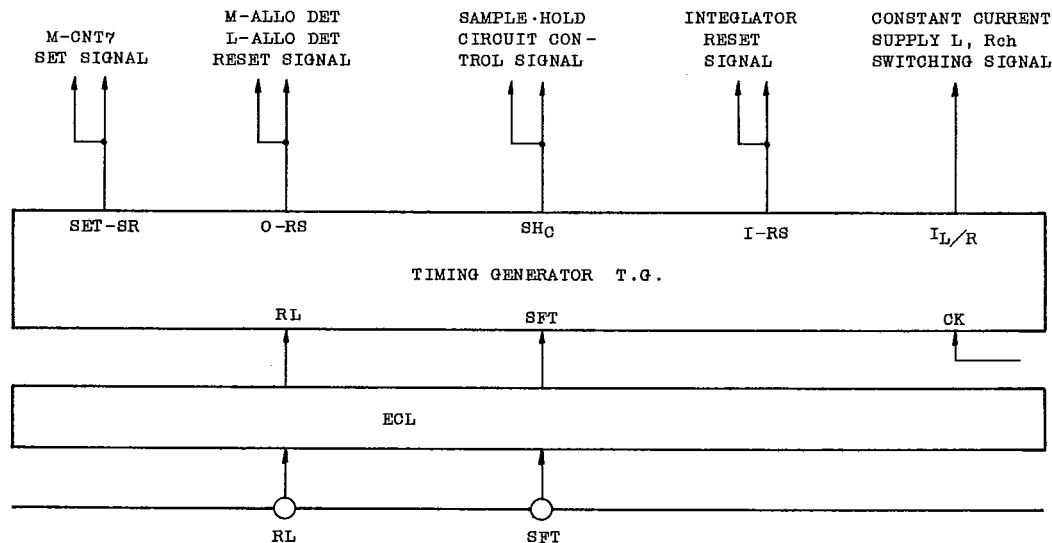


Fig. 5 INPUT AND OUTPUT OF TIMING GENERATOR SIGNALS

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3. CONSTANT CURRENT SUPPLY CIRCUIT: CS128

The constant current supply unit is composed of two constant current supplies: I_{M7} for MSB side 7 bits, and I_{L7} for LSB side 7 bits. By means of designing the current ratio of I_{M7} and I_{L7} as 128:1, and using I_{M7} combined with the counter M-CNT7 and I_{L7} with the counter L-CNT7, the coefficient corresponding to the set data for the counter is converted into the integration period. The counting number 1 of MSB side counter M-CNT7 is made corresponded to the counting number 128 of LSB side counter-CNT7. By using I_{M7} and I_{L7} at the same time, the following expression is obtained instead of the conventional single slope single integration system, and the alternative output of PCM digital audio 16-bits data (14-bits accuracy) is made possible in 44kHz with $f_{OSC} \approx 17\text{MHz}$.

$$\text{Max. counting number ratio} = \frac{2^7}{2^{16}} = \frac{1}{512}$$

The constant current supplies I_{M7} and I_{L7} carry out ON/OFF of SW- C_M and SW- C_L with the control signal which is output from the counter all 0 detection circuits M-ALLO DET and L-ALLO DET of the control block in Fig. 2.

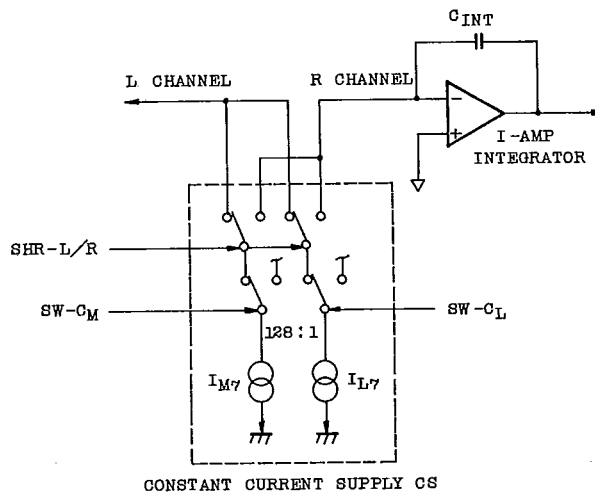


Fig. 6 CONFIGURATION OF CONSTANT CURRENT SUPPLY

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4. INTEGRATION CIRCUIT

The integration circuit is composed of built-in ope.-amp. and external C_{INT}. The period of t₀~t₂ in Fig.8 is the period for charging to C_{INT} by (integrating operation) the constant current supply I_{M7} and I_{L7} in the integration circuit in Fig.7 and for counting and voltage conversion (DA conversion). The integration period is determined by either value of larger one stored in the counter M-CNT7 or L-CNT7 of the control block and is determined as follows.

$$V_{10} = \frac{1}{C_{INT}} \cdot (I_{M7} \cdot N_M + I_{L7} \cdot N_L) \cdot T_{OSC} + V_{reset}$$

- N_M : M-CNT counting number
- N_L : L-CNT counting number
- T_{OSC} : Oscillation output f_{OSC} cycle
- V_{reset}: Reset voltage

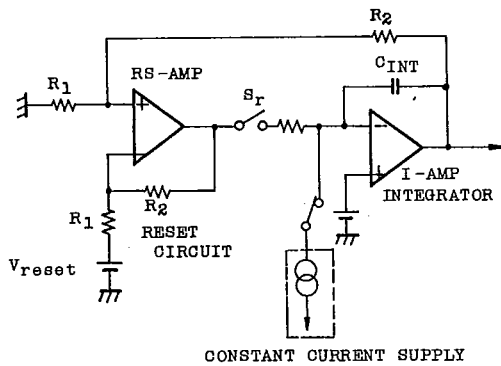


Fig. 7 INTEGRATION CIRCUIT

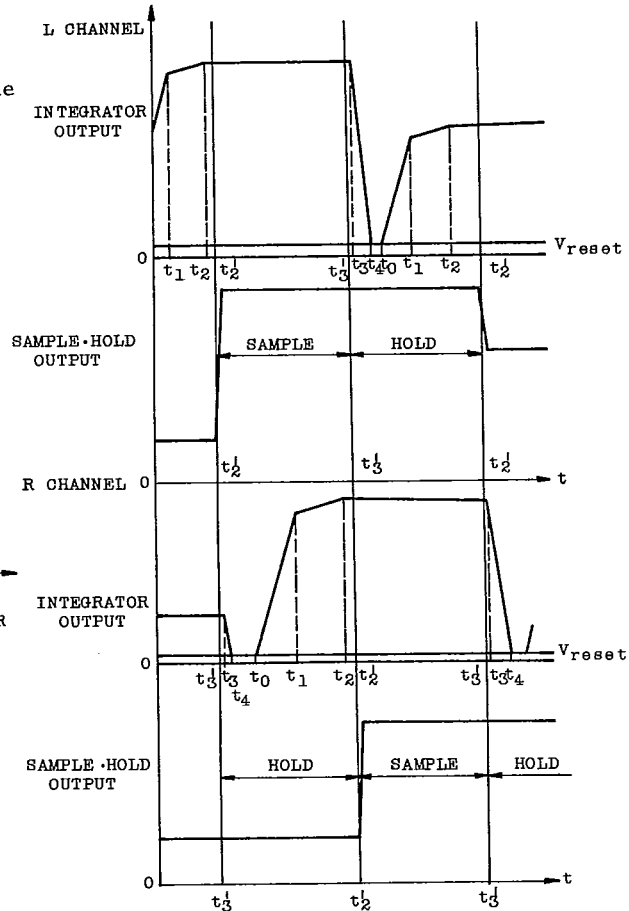


Fig. 8 INTEGRATOR OUTPUT, SAMPLE-HOLD OUTPUT VARIATION

5. SAMPLE·HOLD CIRCUIT

This circuit sample-holds the stabilized voltage during the period of $t_2^1-t_3^1$ and outputs the voltage outside. At t_2^1 , S_1 is made OFF and S_2 ON to start the sampling. At t_3^1 , S_1 is made ON and S_2 OFF, and the sampling voltage is hold.

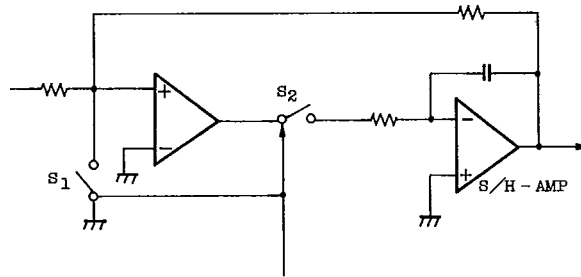


Fig. 9 SAMPLE·HOLD CIRCUIT

6. RESET CIRCUIT

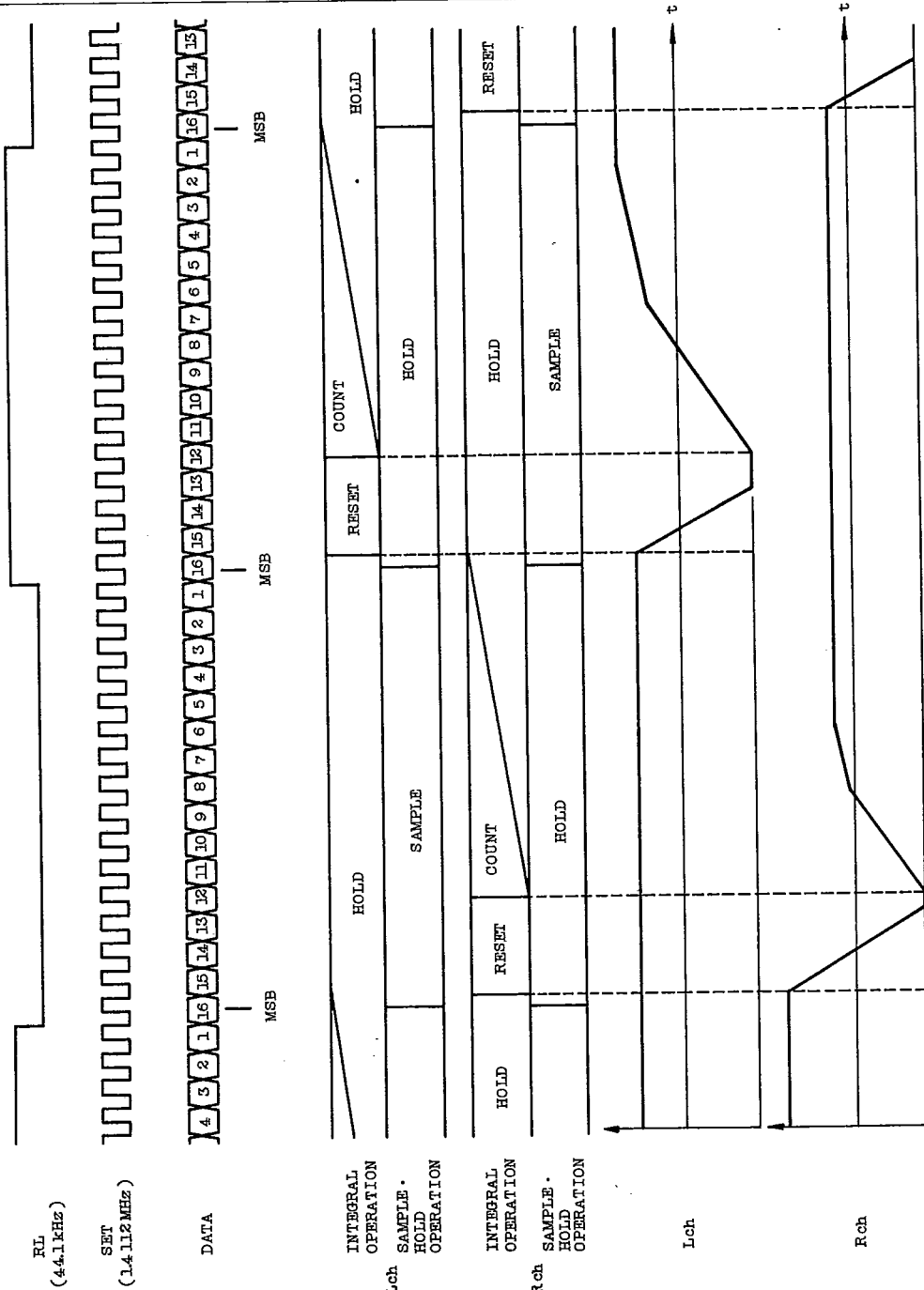
During the period of t_3-t_4 , S_r of the integration circuit in Fig.7 is made ON and the integration capacitor C_{INT} is discharged.

Until the balanced state of $V_0(\text{reset})=V_r$ is obtained, discharge is carried out with the reset amplifier RS-AMP.

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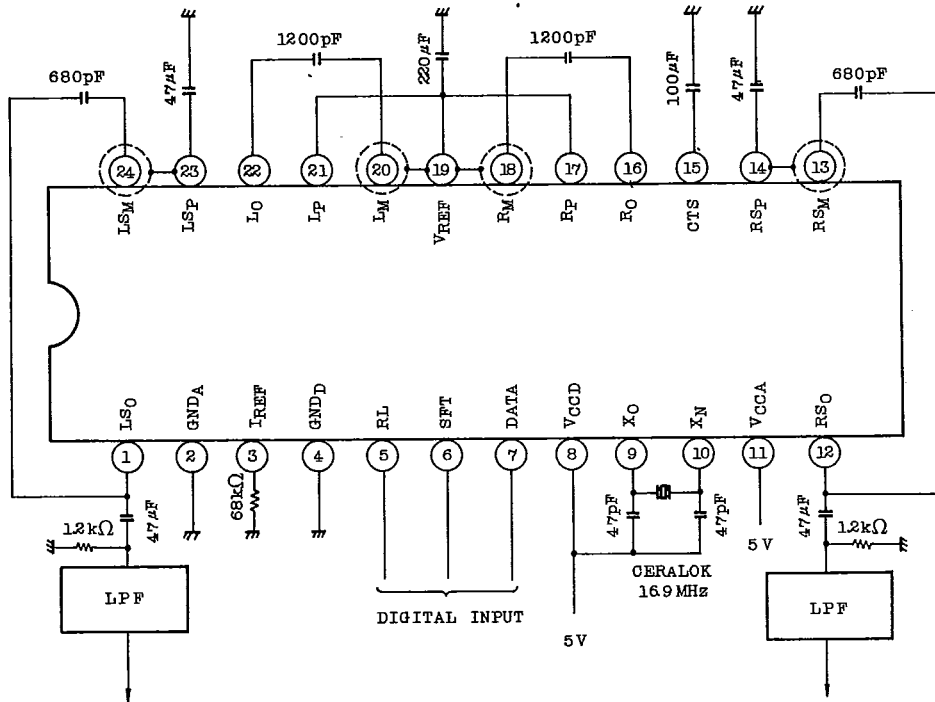
TIMING CHART



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EXAMPLE OF APPLICATION CIRCUIT



- Note 1. To improve characteristics, form the guard ring pattern for pins 13,18,20,24 as shown in the circuit above.
2. Use polystyrol capacitor (precision: within $\pm 3\%$) for integrated capacitor.
 3. Connect the capacitor to V_{CCA}-G_{NDA} and V_{CCD}-G_{NDD} against high frequency noise. Capacitor is 0.0039μF or so.
 4. External constant is the standard value.

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Graph Total harmonic distortion (THD) characteristic (Standard sample used.)
 . Application circuit applied. . LPF: 9th filter applied.

