BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC1032H

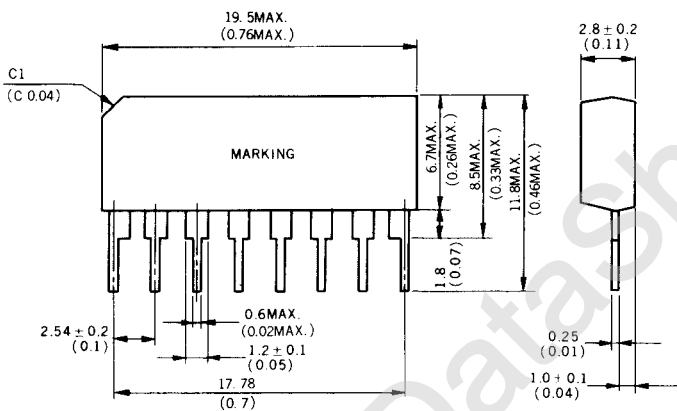## DUAL LOW NOISE PREAMPLIFIER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

The μPC1032H is a silicon monolithic integrated circuit designed for use as a 2 channel preamplifier for a car stereo set. The device has features of low noise, high gain, high output voltage and wide supply voltage range.

Especially, as an advanced production process is used, the device has an excellent feature of very low pulsive noise.

An internal voltage regulator circuit permits the μPC1032H to operate satisfactorily over wide variation of supply voltage.
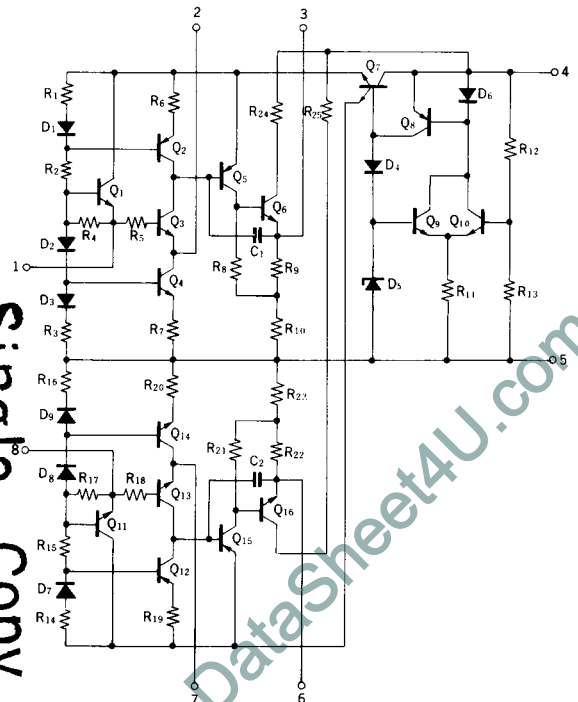
PACKAGE DIMENSIONS

in millimeters (inches)

CONNECTION DIAGRAM

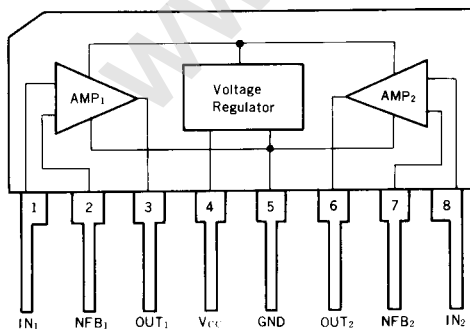| IN$_1$ | NFB$_1$ | OUT$_1$ | V$_{cc}$ | GND | OUT$_2$ | NFB$_2$ | IN$_2$ |

003545

FEATURES

- Two channel
- Wide supply voltage range
- Minimum number of external parts required
- Low noise, especially low pulsive noise
- SIP assures easy mounting on printed circuit board.

EQUIVALENT CIRCUIT

Nippon Electric Co.,Ltd.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Supply Voltage	V_{CC}	18	V
Package Dissipation	P_D	270*	mW
Operating Temperature	T_{opt}	-20 to +75	°C
Storage Temperature	T_{stg}	-40 to +125	°C

*Ta = 75°C

RECOMMENDED CONDITIONS (Ta = 25°C)

Operating Supply Voltage	V_{CC}	13.2	V
Supply Voltage Range	V_{CC}	8 to 17	V
Operating Ambient Temperature		-20 to +75	°C
Load impedance		10 kΩ TYP.	

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 13.2V, f = 1 kHz, R_L = 10 kΩ)

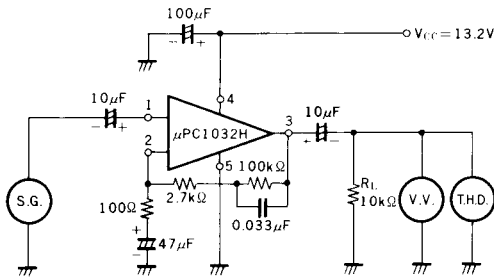| CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CIRCUIT	TEST CONDITIONS
Circuit Current	I_{CC}		7	11.0	mA	①	$v_{in} = 0$
Open Loop Voltage Gain	A_{vo}	70	81		dB	①	$v_O = 0.3V$
Voltage Gain	A_v	33.5	35	35.5	dB	②	$v_O = 0.3V$, $R_{NF} = 1.8 kΩ$
Maximum Output Voltage	V_{OM}	1.1	1.7		V	③	T.H.D. = 1%, NAB ≒ 35 dB
Total Harmonic Distortion	T.H.D.		0.1	0.3	%	③	$v_O = 0.3V$, NAB ≒ 35 dB
Input Impedance	r_i	50	100		kΩ	③	
Equivalent Input Noise Voltage	v_{nin}		1.4	2.0	μVr.m.s.	④	$R_G = 2.2kΩ$, NAB ≒ 35 dB
Cross Talk			-62		dB	⑤	$v_O = 1V$, (The other channel $v_{in} = 0$, $R_G = 2.2kΩ$)
Channel Balance		-0.3	0	+0.3	dB	⑤	$v_O = 0.3V$

TEST CIRCUITS

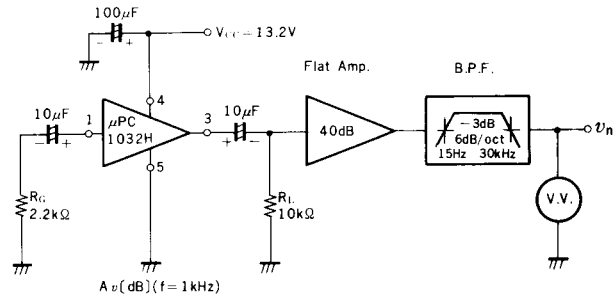### ① I_{CC}, A_{vo} Test Circuit

② A_v Test Circuit (for Ch. 1)

2

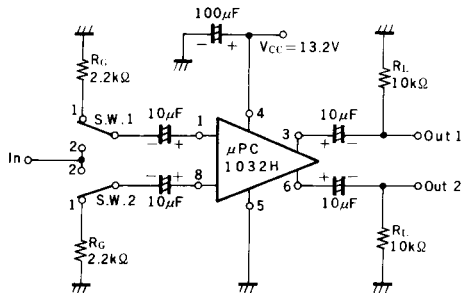③ V$_{OM}$, T.H.D., r$_i$ Test Circuit
(for Ch. 1)

④ v$_{nin}$ Test Circuit
(for Ch. 1)

v$_{nin}$ is calculated by v$_n$ and amp. gain (A$_v$ +40 dB).
External components of the IC are the same as the Test Circuit ③

⑤ Cross Talk, Channel Balance Test Circuit

External Components of the IC are the same as the Test Circuit ③
Cross talk Test Procedure
    20 log Out$_2$/Out$_1$
    Switch Position   SW$_1$ → 2, SW$_2$ → 1
    20 log Out$_1$/Out$_2$
    Switch Position   SW$_1$ → 1, SW$_2$ → 2
Channel Balance Test Procedure
    20 log Out$_1$/Out$_2$
    Switch Position   SW$_1$ → 2, SW$_2$ → 2

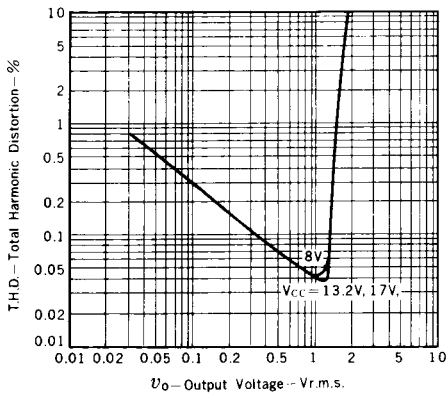# TYPICAL CHARACTERISTICS (Ta = 25°C)

OUTPUT VOLTAGE vs.
INPUT VOLTAGE
(Test Circuit ③)

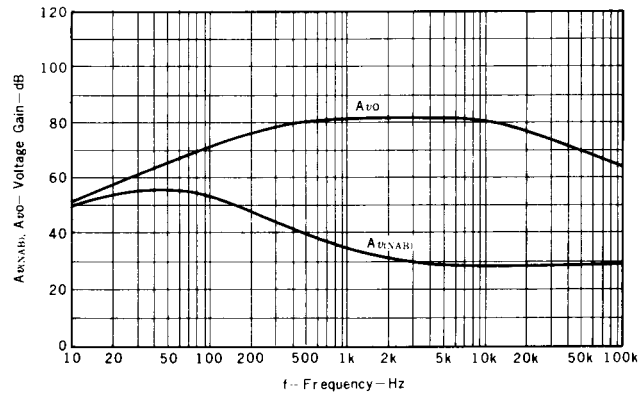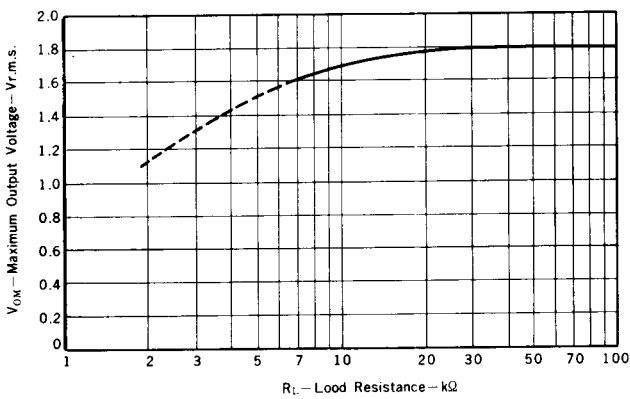TOTAL HARMONIC DISTORTION vs.
OUTPUT VOLTAGE
(Test Circuit ③)

3

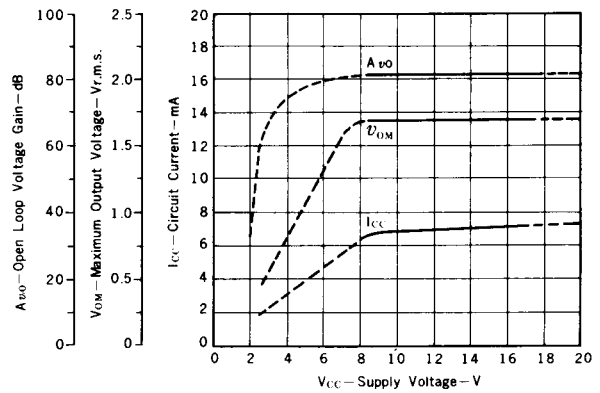**TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE**
(Test Circuit ③)

T.H.D.— Total Harmonic Distortion — %

v_o — Output Voltage — Vr.m.s.

8V

V_{CC} = 13.2V, 17V

VOLTAGE GAIN vs. FREQUENCY
(Test Circuit ① , ③)

$A_{V(NAB)}$, A_{VO} — Voltage Gain — dB

A_{VO}

$A_{V(NAB)}$

f — Frequency — Hz

MAXIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE
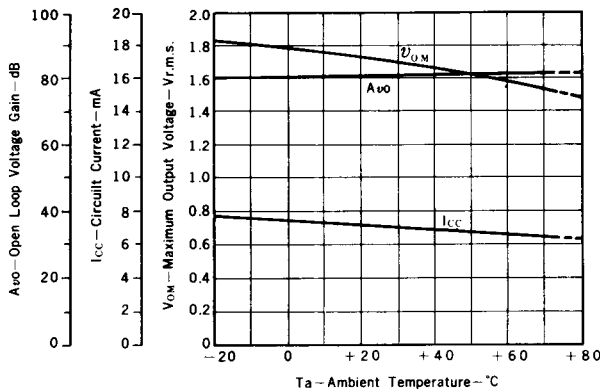(Test Circuit ③)

V_{OM} — Maximum Output Voltage — Vr.m.s.

R_L — Load Resistance — kΩ

CIRCUIT CURRENT, MAXIMUM OUTPUT VOLTAGE, OPEN LOOP VOLTAGE GAIN vs. SUPPLY VOLTAGE
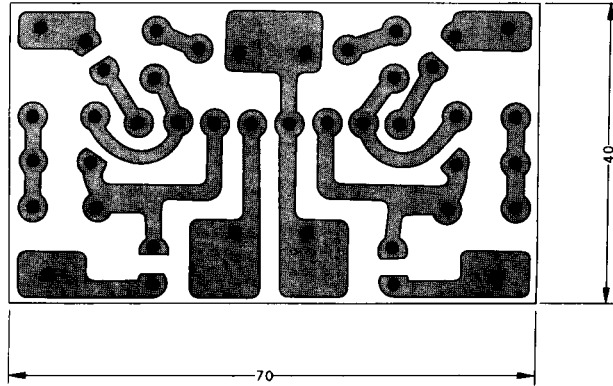(Test Circuit ① , ③)

A_{VO} — Open Loop Voltage Gain — dB

V_{OM} — Maximum Output Voltage — Vr.m.s.

I_{CC} — Circuit Current — mA

A_{VO}

v_{OM}

I_{CC}

V_{CC} — Supply Voltage — V

CIRCUIT CURRENT, MAXIMUM OUTPUT VOLTAGE, OPEN LOOP VOLTAGE GAIN AMBIENT TEMPERATURE
(Test Circuit ① , ③)

A_{VO} — Open Loop Voltage Gain — dB

I_{CC} — Circuit Current — mA

V_{OM} — Maximum Output Voltage — Vr.m.s.

v_{OM}

A_{VO}

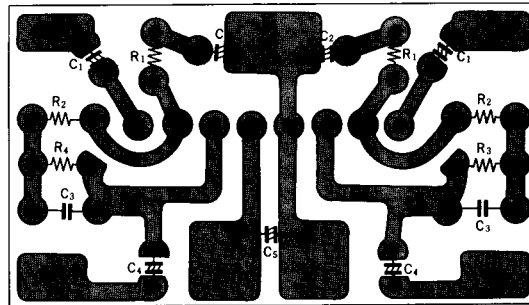I_{CC}

Ta — Ambient Temperature — °C

TYPICAL PRINTED CIRCUIT BOARD PATTERN

Bottom View (Unit : millimeters)

Components Layout

Foil Side

Components Side

100μF(16V)
C5

Vcc

C1 1/8
IN
10μF
(6.3V)

2/7

μPC1032H

4

3/6

C4
10μF
(10V)

OUT

5

100kΩ
R3

R2
2.7kΩ

C3 0.033μF

R1
100Ω

47μF
(6.3V)
C2