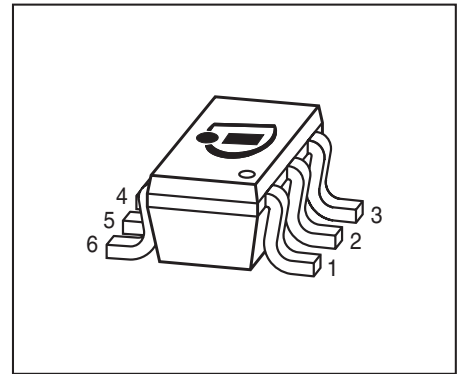
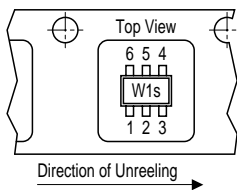


NPN Silicon AF Transistor Array

- For AF stages and driver applications
- High current gain
- Low collector-emitter saturation voltage
- Two (galvanic) internal isolated NPN/PNP transistors in one package
- Pb-free (RoHS compliant) package
- Qualified according AEC Q101

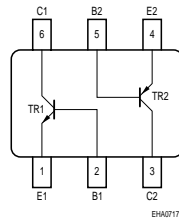


Tape loading orientation



Marking on SC74 package (for example W1s) corresponds to pin 1 of device

Position in tape: pin 1 opposite of feed hole side



SC74_Tape

Type	Marking	Pin Configuration						Package
BC817UPN	1Bs	1=E1	2=B1	3=C2	4=E2	5=B2	6=C1	SC74

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	45	V
Collector-base voltage	V_{CBO}	50	
Emitter-base voltage	V_{EBO}	5	
Collector current	I_C	500	mA
Peak collector current, $t_p \leq 10$ ms	I_{CM}	1000	
Base current	I_B	100	
Peak base current	I_{BM}	200	mW
Total power dissipation- $T_S \leq 115$ °C	P_{tot}	330	
Junction temperature	T_j	150	
Storage temperature	T_{stg}	-65 ... 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point ¹⁾	R_{thJS}	≤ 105	K/W

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

DC Characteristics

Collector-emitter breakdown voltage $I_C = 10 \text{ mA}, I_B = 0$	$V_{(BR)CEO}$	45	-	-	V
Collector-base breakdown voltage $I_C = 10 \mu\text{A}, I_E = 0$	$V_{(BR)CBO}$	50	-	-	
Emitter-base breakdown voltage $I_E = 10 \mu\text{A}, I_C = 0$	$V_{(BR)EBO}$	5	-	-	
Collector-base cutoff current $V_{CB} = 25 \text{ V}, I_E = 0$ $V_{CB} = 25 \text{ V}, I_E = 0, T_A = 150^\circ\text{C}$	I_{CBO}	-	-	0.1 50	μA
Emitter-base cutoff current $V_{EB} = 4 \text{ V}, I_C = 0$	I_{EBO}	-	-	100	nA
DC current gain ²⁾ $I_C = 100 \text{ mA}, V_{CE} = 1 \text{ V}$ $I_C = 300 \text{ mA}, V_{CE} = 1 \text{ V}$	h_{FE}	160 100	250 -	400 -	-
Collector-emitter saturation voltage ²⁾ $I_C = 500 \text{ mA}, I_B = 50 \text{ mA}$	V_{CEsat}	-	-	0.7	V
Base emitter saturation voltage ²⁾ $I_C = 500 \text{ mA}, I_B = 50 \text{ mA}$	V_{BEsat}	-	-	1.2	

AC Characteristics

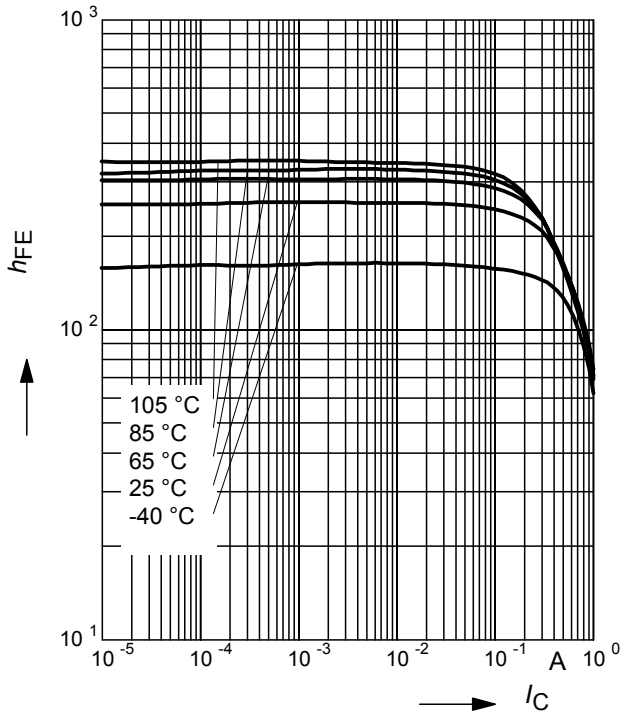
Transition frequency $I_C = 50 \text{ mA}, V_{CE} = 5 \text{ V}, f = 100 \text{ MHz}$	f_T	-	170	-	MHz
Collector-base capacitance $f = 1 \text{ MHz}, V_{BE} = 10 \text{ V}$	C_{cb}	-	6	-	pF
Emitter-base capacitance $V_{EB} = 0.5 \text{ V}, f = 1 \text{ MHz}$	C_{eb}	-	60	-	

¹⁾For calculation of R_{thJA} please refer to Application Note AN077 (Thermal Resistance Calculation)

²⁾Pulse test: $t < 300\mu\text{s}; D < 2\%$

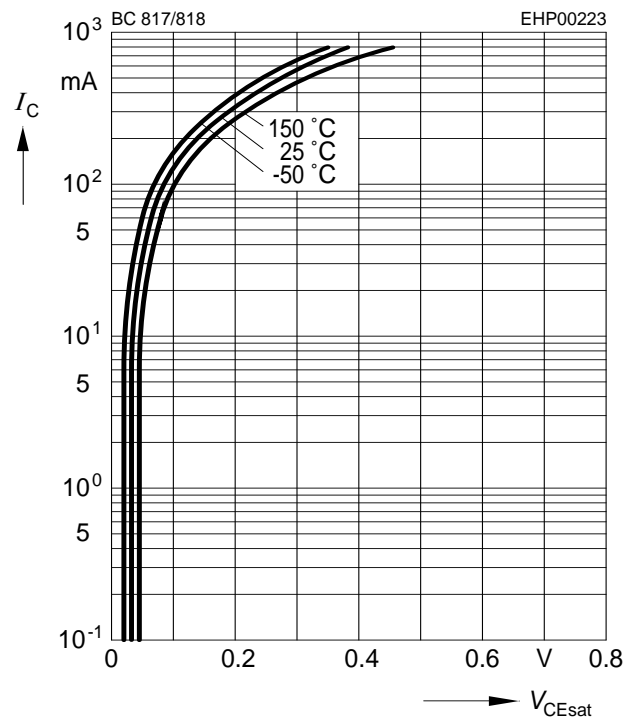
DC current gain $h_{FE} = f(I_C)$

$V_{CE} = 1\text{ V}$



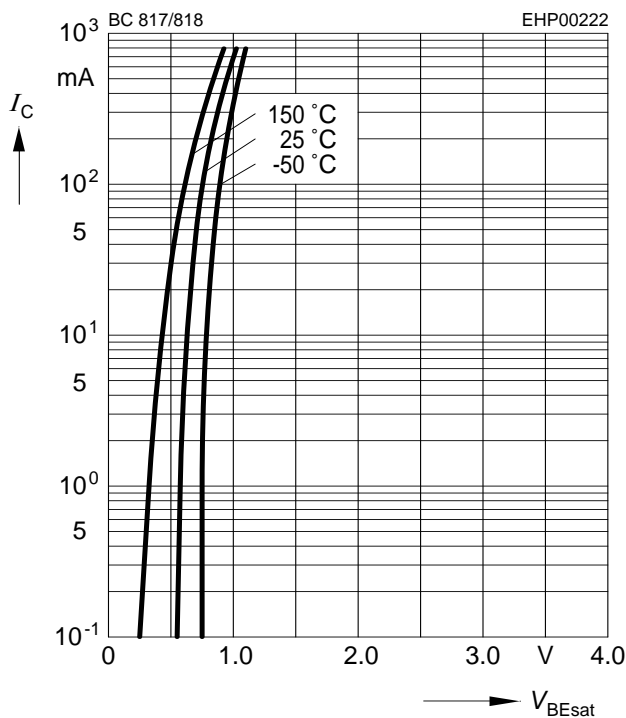
Collector-emitter saturation voltage

$I_C = f(V_{CEsat}), h_{FE} = 10$



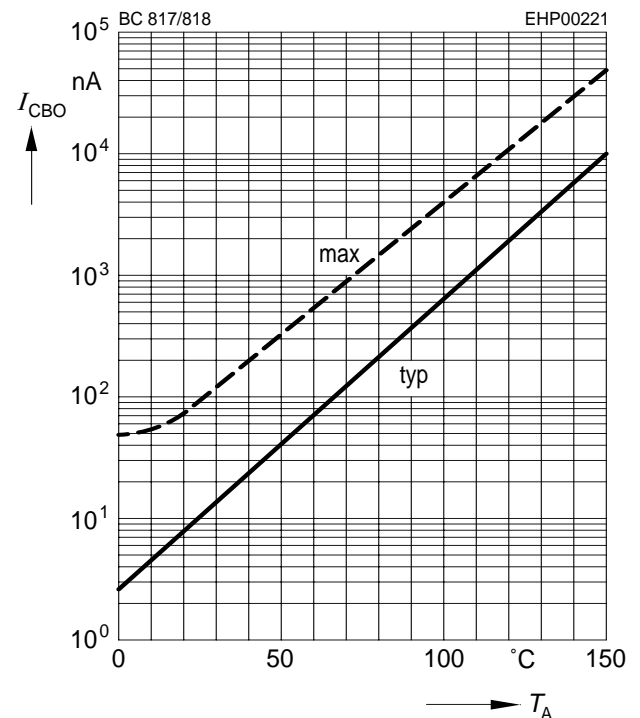
Base-emitter saturation voltage

$I_C = f(V_{BEsat}), h_{FE} = 10$



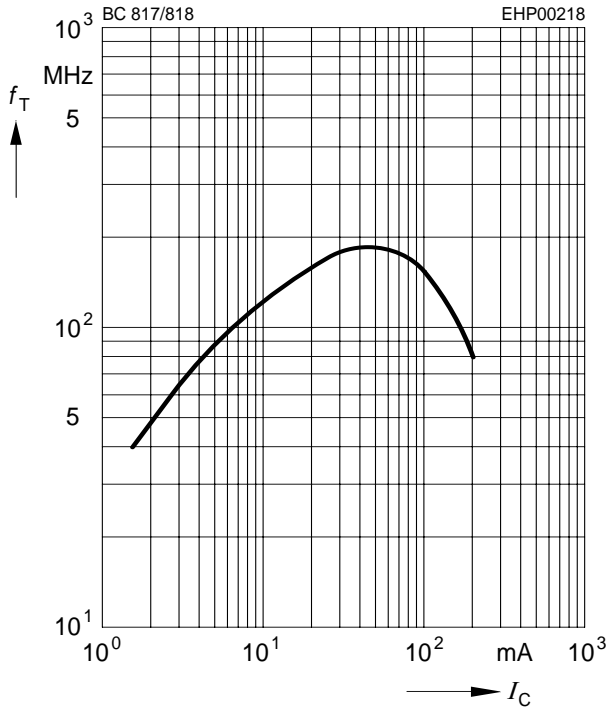
Collector cutoff current $I_{CBO} = f(T_A)$

$V_{CBO} = 25\text{ V}$



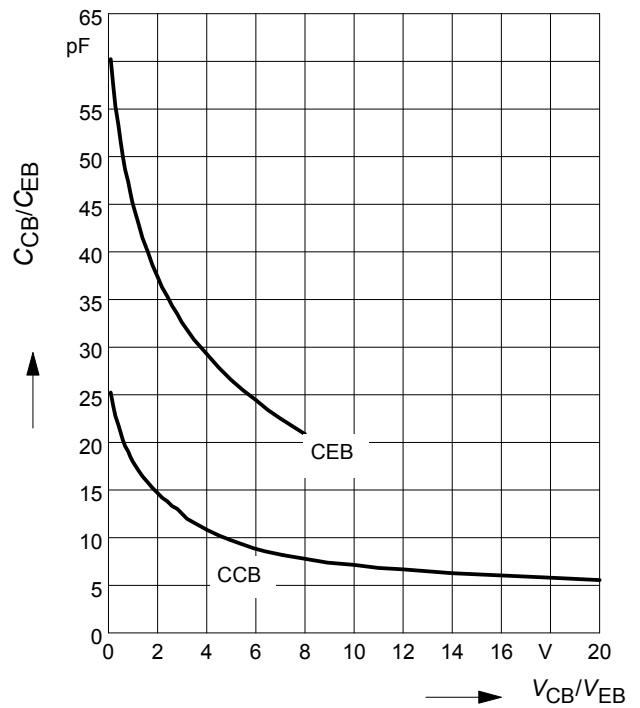
Transition frequency $f_T = f(I_C)$

V_{CE} = parameter in V, $f = 2$ GHz



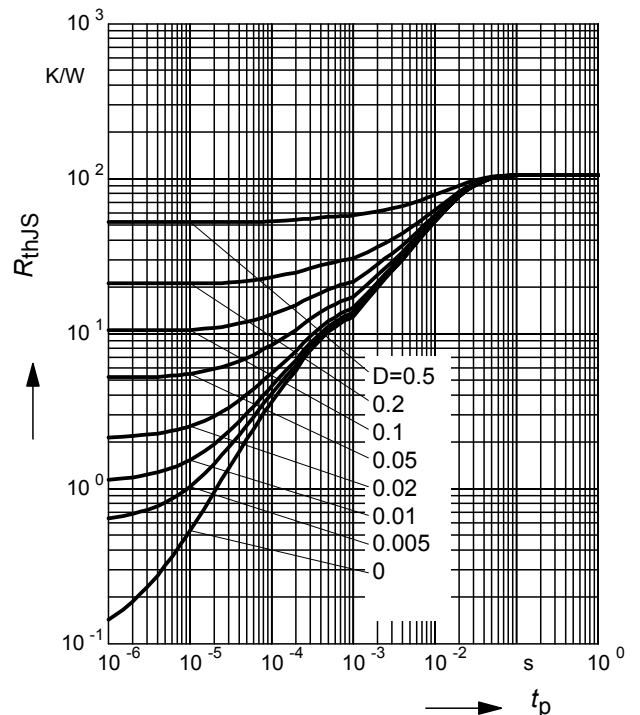
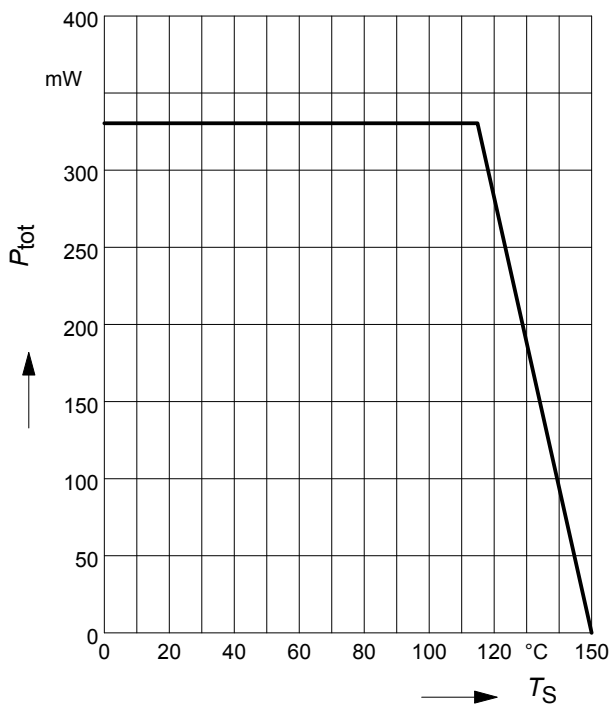
Collector-base capacitance $C_{cb} = f(V_{CB})$

Emitter-base capacitance $C_{eb} = f(V_{EB})$



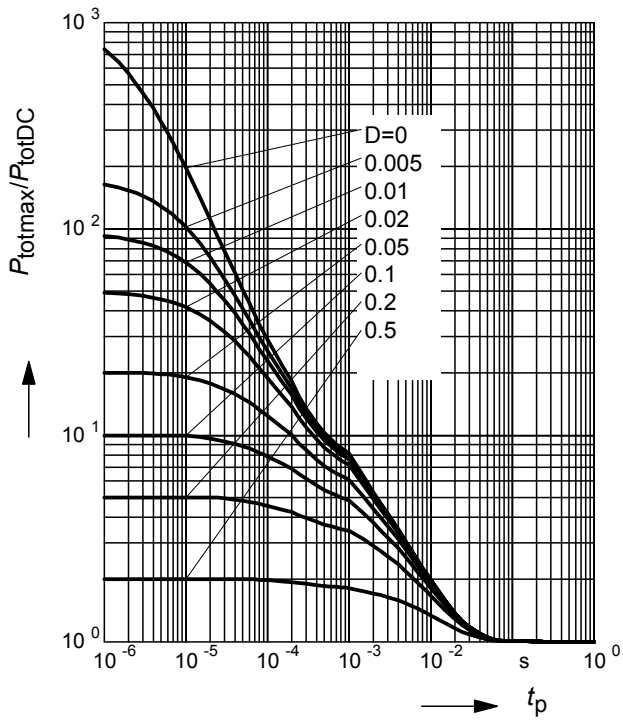
Total power dissipation $P_{tot} = f(T_S)$

Permissible Pulse Load $R_{thJS} = f(t_p)$

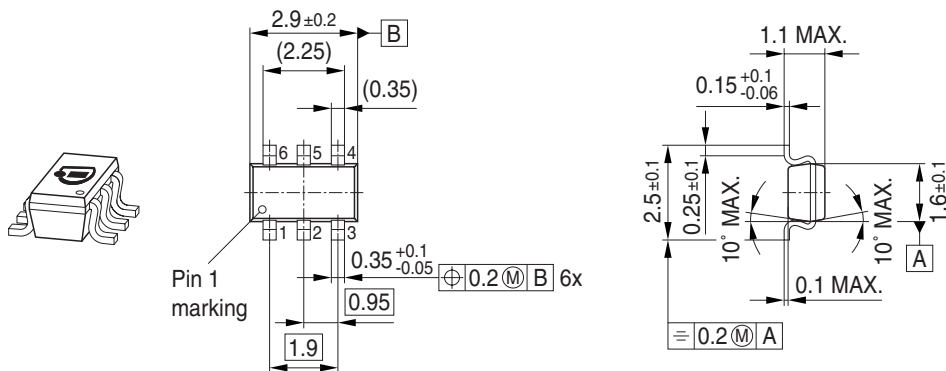


Permissible Pulse Load

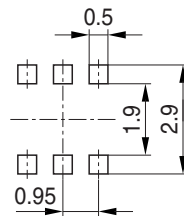
$$P_{\text{totmax}}/P_{\text{totDC}} = f(t_p)$$



Package Outline

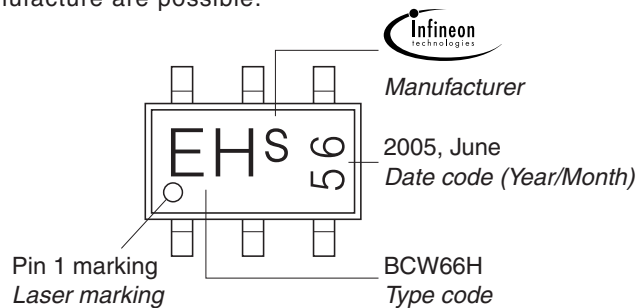


Foot Print



Marking Layout (Example)

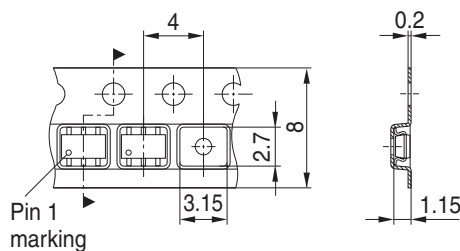
Small variations in positioning of Date code, Type code and Manufacture are possible.



Standard Packing

Reel \varnothing 180 mm = 3.000 Pieces/Reel
 Reel \varnothing 330 mm = 10.000 Pieces/Reel

For symmetric types no defined Pin 1 orientation in reel.



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