

## 6N137-L

### High CMR, High Speed TTL Compatible Optocouplers

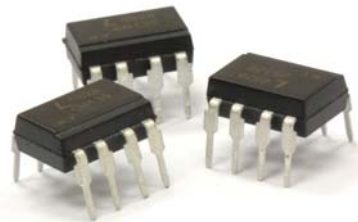


Dec.2008

#### Description

The 6N137-L consists of a high efficient AlGaAs Light Emitting Diode and a high speed optical detector. This design provides excellent AC and DC isolation between the input and output sides of the Optocoupler. The output of the optical detector features an open collector Schottky clamped transistor. The enable function allows the optical detector to be strobed. The internal shield ensures high common mode transient immunity. A guaranteed common mode transient immunity is up to 15,000V/μs.

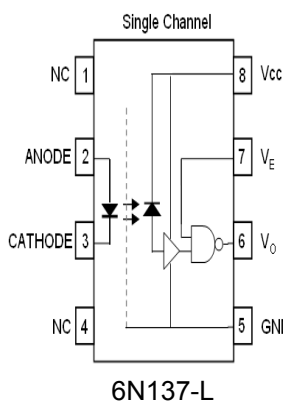
The Optocoupler operational parameters are guaranteed over the temperature range from -40°C ~ +85°C.



#### Features

- High speed – 10MBd typical
- Guaranteed AC and DC performance over temperature -40°C ~ +85°C.
- LSTTL/TTL Compatible.
- Available in Dual-in-line, Wide lead spacing, Surface mounting package.
- Storable output.
- UL, CSA, IEC/EN/DIN EN60747-5-2 – Pending

#### Functional Diagram



Truth Table (Positive Logic)

LED	ENABLE	OUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H
ON	NC	L
OFF	NC	H

A 0.1μF bypass Capacitor must be connected between Pin8 and Pin5

#### Application

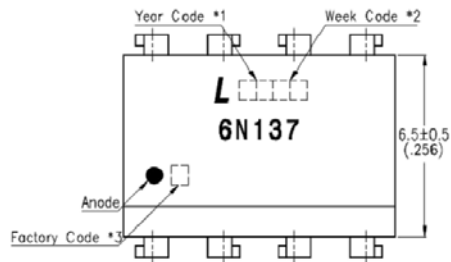
- High Voltage Isolation
- Isolation in line receivers
- Ground loop elimination
- Feedback Element in Switching Mode Power Supplier
- High Speed Logic Ground Isolation – TTL/TTL, TTL/CMOS, TTL/LSTTL
- Pulse transformer replacement
- Power transistor isolation in motor drives
- Interface between Microprocessor system, computer and their peripheral

## Ordering Information

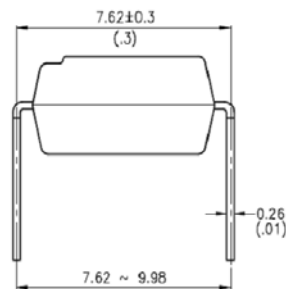
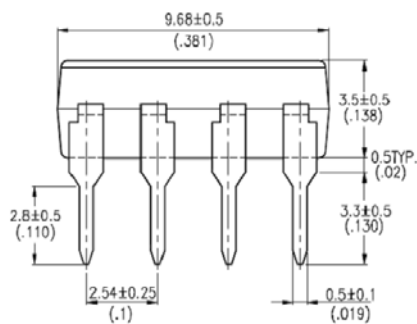
Part	Option	Minimum CMR		Input-On Current (mA)	Output Enable	Remarks
		dV/dt (V/ $\mu$ s)	V <sub>CM</sub> (V)			
6N137	-L					Single Channel, DIP-8
	M-L	1,000	20	5	YES	Single Channel, Wide Lead Spacing
	S-L					Single Channel, SMD-8

## Package Dimensions

### 8-pin DIP Package (6N137-L)

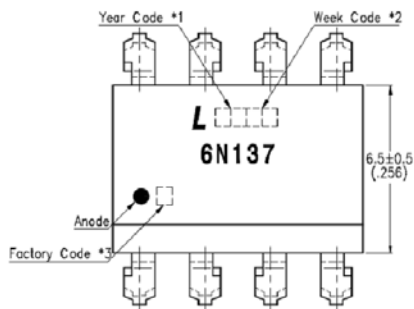


- \*1. Year date code.
  - \*2. 2-digit work week.
  - \*3. Factory identification mark  
(Z : Taiwan, Y : Thailand).
- Dimensions are in Millimeters and (Inches).

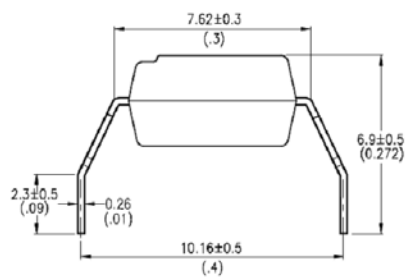
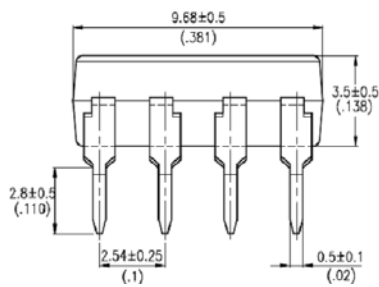


## Package Dimensions

### 8-pin DIP Wide Lead Spacing Package (6N137M-L)

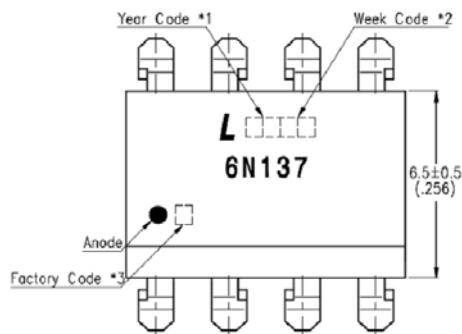


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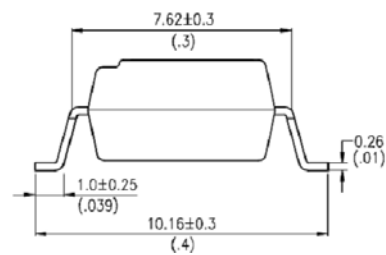
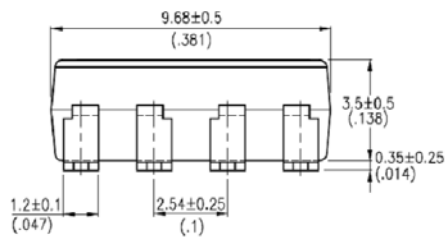


### Package Dimensions

#### 8-pin DIP Surface Mount Package (6N137S-L)

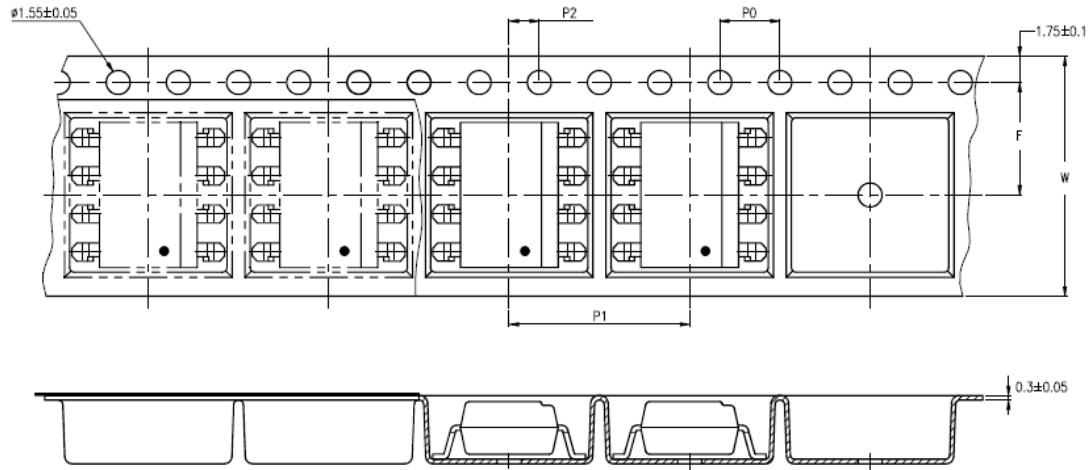


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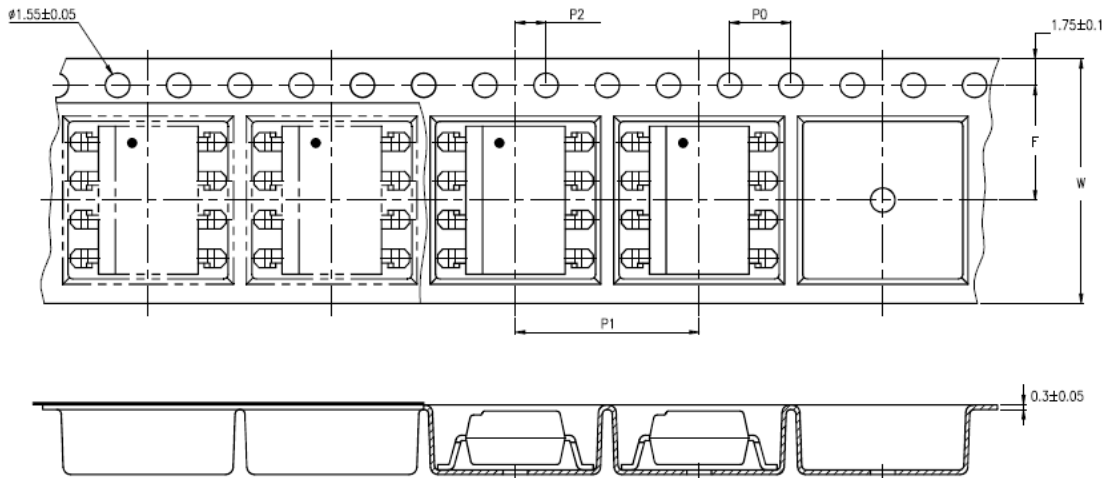


## Taping Dimensions

### 6N137S-TA-L

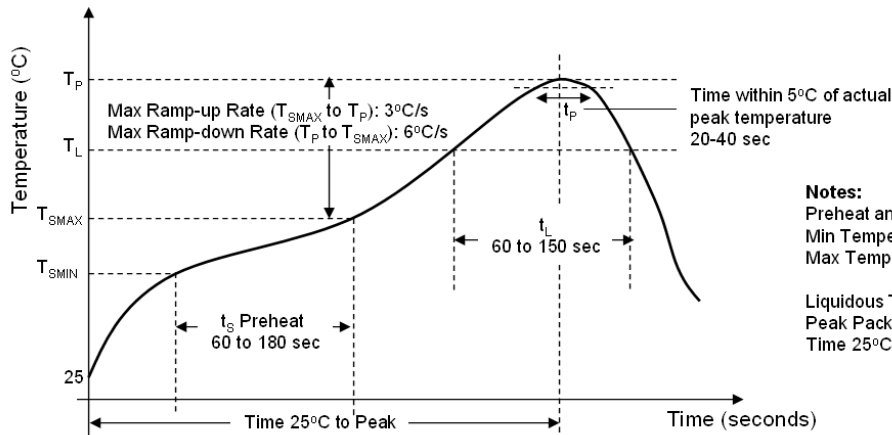


### 6N137S-TA1-L



Description	Symbol	Dimensions in millimeters ( inches )
Tape wide	W	$16 \pm 0.3$ ( .63 )
Pitch of sprocket holes	P0	$4 \pm 0.1$ ( .15 )
Distance of compartment	F	$7.5 \pm 0.1$ ( .295 )
Distance of compartment to compartment	P1	$2 \pm 0.1$ ( .079 )
Distance of compartment to compartment	P1	$12 \pm 0.1$ ( .472 )

## Recommended Lead Free Reflow Profile



**Notes:**

Preheat and Soak:

Min Temperature ( $T_{S_{MIN}}$ ) = 150°C

Max Temperature ( $T_{S_{MAX}}$ ) = 200°C

Liquidous Temperature ( $T_L$ ) = 217°C

Peak Package Body Temperature = 260°C

Time 25°C to Peak Temperature = 8 minutes max.

## Absolute Maximum Ratings\*1

Parameter	Symbol	Min	Max	Units	Note
Storage Temperature	$T_{ST}$	-55	125	°C	
Operating Temperature	$T_A$	-40	85	°C	
Isolation Voltage	$V_{ISO}$		5000	$V_{RMS}$	
Supply Voltage	$V_{CC}$		7	V	
Lead Solder Temperature * 2			260	°C	
<b>Input</b>					
Average Forward Input Current	$I_F$		20	mA	2
Reverse Input Voltage	$V_R$		5	V	
Input Power Dissipation	$P_I$		40	mW	
Enable Input Voltage	$V_E$		$V_{CC}+0.5$	V	
Enable Input current	$I_E$		5	mA	
<b>Output</b>					
Output Collector Current	$I_O$		50	mA	
Output Collector Voltage	$V_O$		7	V	
Output Collector Power Dissipation	$P_O$		85	mW	

1. Ambient temperature = 25°C, unless otherwise specified. Stresses exceeding the absolute maximum ratings can cause permanent damage to the device. Exposure to absolute maximum ratings for long periods of time can adversely affect reliability.

2. 260°C for 10 seconds. Refer to Lead Free Reflow Profile.



**Recommended Operating Conditions**

Parameter	Symbol	Min	Max	Units
Operating Temperature	$T_A$	-40	85	°C
Supply Voltage	$V_{CC}$	4.5	5.5	V
Low Level Input Current	$I_{FL}$	0	250	μA
High Level Input Current	6N137-L $I_{FH}$	5	15	mA
Low Level Enable Voltage	$V_{EL}$	0	0.8	V
High Level Enable Voltage	$V_{EH}$	2	$V_{CC}$	V
Output Pull-up Resistor	$R_L$	330	4k	Ω
Fan Out (at $R_L=1k\Omega$ per channel)	N		5	TTL Loads

### Electrical Specifications

Parameters	Test Condition	Symbol	Min	Typ	Max	Units	Note
<b>Input</b>							
Input Forward Voltage	$I_F = 10\text{mA}$	$V_F$		1.38	1.70	V	
Input Forward Voltage Temperature Coefficient	$I_F = 10\text{mA}$	$\Delta V_F / \Delta T$		-1.5		mV/°C	
Input Reverse Voltage	$I_R = 10\mu\text{A}$	$BV_R$	5			V	
Input Threshold Current	$V_E = 2\text{V}, V_{CC} = 5.5\text{V}, I_{OL} (\text{sinking}) = 13\text{mA}$	$I_{TH}$		1.35	5	mA	
				2 <sup>(1)</sup>	3	mA	
Input Capacitance	$f = 1\text{MHz}, V_F = 0\text{V}$	$C_{IN}$		34		pF	
<b>Output</b>							
High Level Supply Current	$V_E = 0.5\text{V}, V_{CC} = 5.5\text{V}, I_F = 0\text{mA}$	$I_{CCH}$		7.4	10	mA	
Low Level Supply Current	$V_E = 0.5\text{V}, V_{CC} = 5.5\text{V}, I_F = 10\text{mA}$	$I_{CCL}$		10	13	mA	
High Level Enable Current	$V_E = 2\text{V}$	$I_{EH}$		-0.6	-1.6	mA	
Low Level Enable Current	$V_E = 0.5\text{V}$	$I_{EL}$		-0.9	-1.6	mA	
High Level Enable Voltage		$V_{EH}$	2			V	
Low Level Enable Voltage		$V_{EL}$			0.8	V	
High Level Output Current	$V_E = 2\text{V}, V_{CC} = 5.5\text{V}, V_O = 5.5\text{V}, I_F = 250\mu\text{A}$	$I_{OH}$			100	$\mu\text{A}$	
Low Level Output Voltage	$V_E = 2\text{V}, V_{CC} = 5.5\text{V}, I_F = 5\text{mA}, I_{OL} (\text{sinking}) = 13\text{mA}$	$V_{OL}$		0.25	0.60	V	

Specified over recommended temperature ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ) unless otherwise specified. Typical values applies to  $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$ . See note 1.

### Switching Specifications

Parameter	Test Condition	Symbol	Min	Typ	Max	Units	Note
Propagation Delay Time to High Output Level	$R_L = 350\Omega, C_L = 15\text{pF}$	$t_{PLH}$	25	40	100	ns	3
Propagation Delay Time to Low Output Level	$R_L = 350\Omega, C_L = 15\text{pF}$	$t_{PHL}$	25	27	100	ns	4
Pulse Width Distortion	$R_L = 350\Omega, C_L = 15\text{pF}$	$ t_{PLH} - t_{PHL} $		12		ns	
Propagation Delay Skew	$R_L = 350\Omega, C_L = 15\text{pF}$	$t_{PSK}$					
Output Rise Time (10 to 90%)	$R_L = 350\Omega, C_L = 15\text{pF}$	$t_r$		20		ns	
Output Fall Time (90 to 10%)	$R_L = 350\Omega, C_L = 15\text{pF}$	$t_f$		6.6		ns	
Propagation Delay Time of Enable from $V_{EH}$ to $V_{EL}$	$R_L = 350\Omega, C_L = 15\text{pF}, V_{EL} = 0V, V_{EH} = 3V$	$t_{ELH}$		28		ns	5
Propagation Delay Time of Enable from $V_{EL}$ to $V_{EH}$	$R_L = 350\Omega, C_L = 15\text{pF}, V_{EL} = 0V, V_{EH} = 3V$	$t_{EHL}$		12		ns	6
Logic High Common Mode Transient Immunity	$ V_{CM}  = 20V, V_{CC} = 5V, I_F = 0\text{mA}, V_{O(MIN)} = 2V, R_L = 350\Omega, T_A = 25^\circ\text{C}$	$ CM_H $	1,000			V/ $\mu\text{s}$	7,9
Logic Low Common Mode Transient Immunity	$ V_{CM}  = 20V, V_{CC} = 5V, I_F = 7.5\text{mA}, V_{O(MIN)} = 0V, R_L = 350\Omega, T_A = 25^\circ\text{C}$	$ CM_L $	1,000			V/ $\mu\text{s}$	8,9

Specified over recommended temperature ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ),  $V_{CC} = 5V$ ,  $I_F = 7.5\text{mA}$  unless otherwise specified. Typical values applies to  $V_{CC} = 5V$ ,  $T_A = 25^\circ\text{C}$ .

### Isolation Characteristics

Parameter	Test Condition	Symbol	Min	Typ	Max	Units	Note
Input-Output Insulation Leakage Current	45% RH, t = 5s, V <sub>I-O</sub> = 3kV DC, T <sub>A</sub> = 25°C	I <sub>I-O</sub>			1.0	μA	10,11
Withstand Insulation Test Voltage	RH ≤ 50%, t = 1min, T <sub>A</sub> = 25°C	V <sub>ISO</sub>	5000			V	10,11,12
Input-Output Resistance	V <sub>I-O</sub> = 500V DC	R <sub>I-O</sub>		6.5x10 <sup>11</sup>		Ω	10
Input-Output Capacitance	f = 1MHz, T <sub>A</sub> = 25°C	C <sub>I-O</sub>		1.0		pF	10

Specified over recommended temperature (T<sub>A</sub> = -40°C to +85°C) unless otherwise specified. Typical values applies to T<sub>A</sub> = 25°C

### Notes

1. A 0.1μF or bigger bypass capacitor for V<sub>CC</sub> is needed as shown in Fig.1
2. Peaking driving circuit may be used to speed up the LED. The peak drive current of LED may go up to 50mA and maximum pulse width 50ns, as long as average current doesn't exceed 20mA.
3. t<sub>PLH</sub> (propagation delay) is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
4. t<sub>PHL</sub> (propagation delay) is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
5. The t<sub>ELH</sub> enable propagation delay is measured from the 1.5 V point on the falling edge of the enable input pulse to the 1.5 V point on the rising edge of the output pulse.
6. The t<sub>EHL</sub> enable propagation delay is measured from the 1.5 V point on the rising edge of the enable input pulse to the 1.5 V point on the falling edge of the output pulse.
7. CM<sub>H</sub> is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., VO > 2.0 V).
8. CM<sub>L</sub> is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., VO < 0.8 V).
9. No external pull up is required for a high logic state on the enable input. If the enable pin is not used, tying it to V<sub>CC</sub>.
10. Device is considered a two-terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
11. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage 3000 V rms for one second (leakage current less than 5 uA). This test is performed before the 100% production test for partial discharge
12. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage 6000 V rms for one second (leakage current less than 5 uA). This test is performed before the 100% production test for partial discharge

## Switching Time Test Circuit

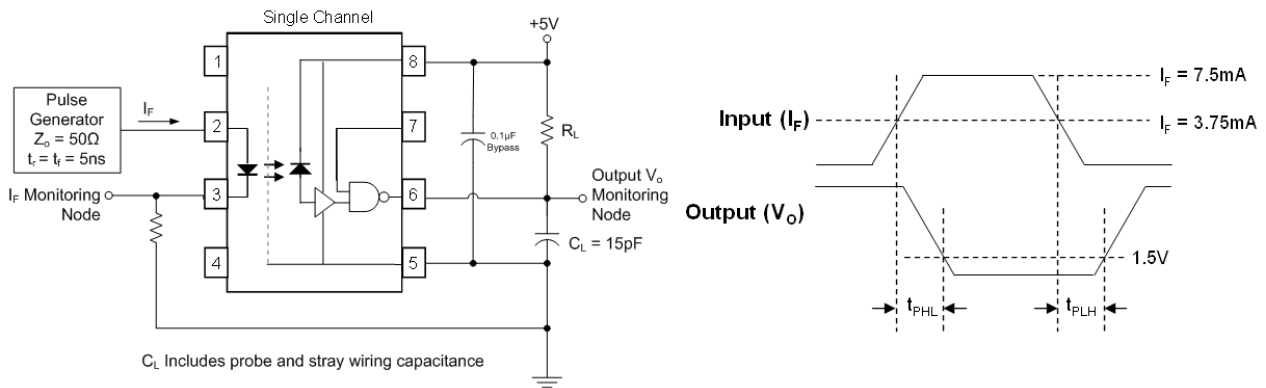


Figure 1: Single Channel Test Circuit for  $t_{PHI}$  and  $t_{PLH}$

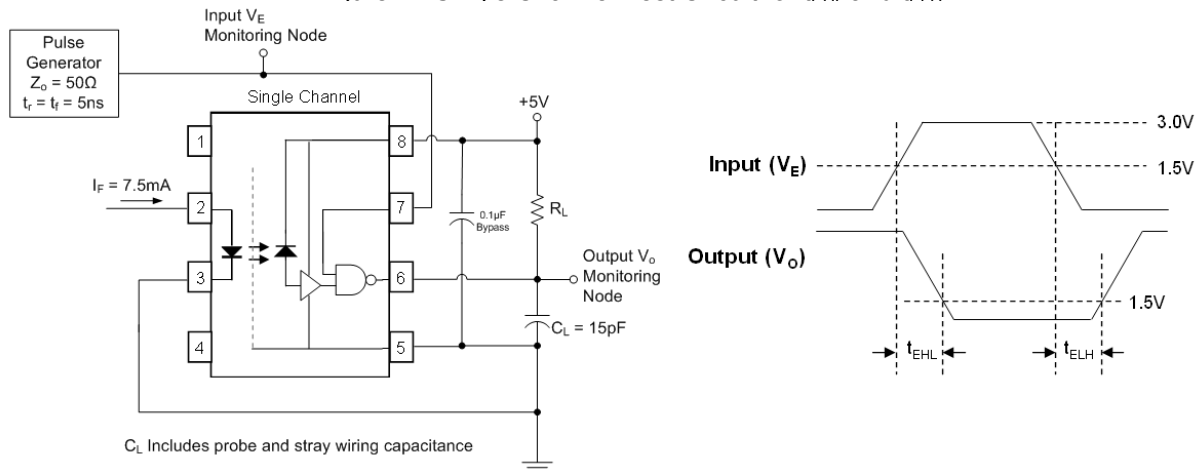


Figure 2: Single Channel Test Circuit for  $t_{EHL}$  and  $t_{ELH}$

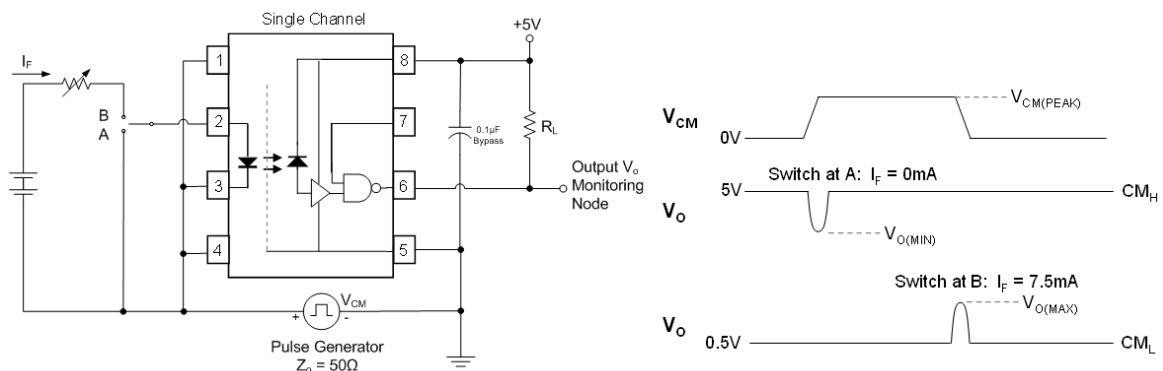


Figure 3: Single Channel Test Circuit for Common Mode Transient Immunity

## Characteristics Curves

Figure 4: Typical Input Diode Forward Characteristics

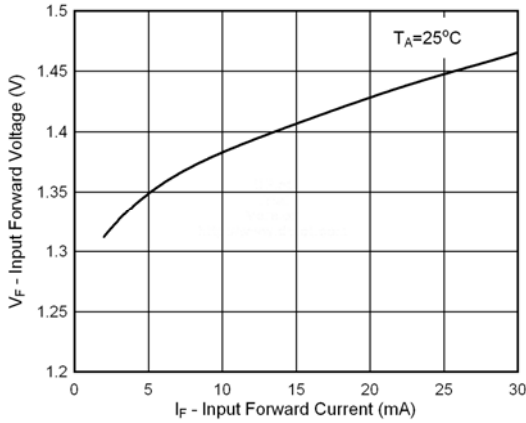


Figure 7: Typical Output Voltage vs. Input Forward Current

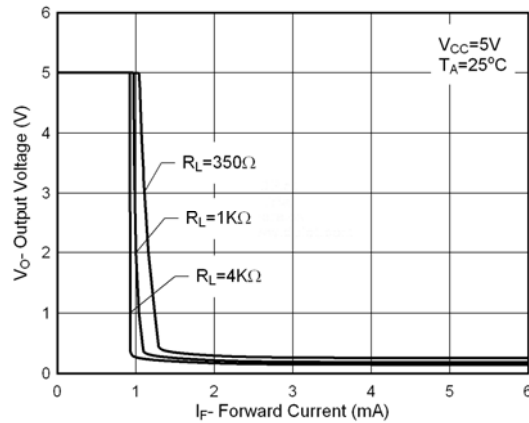


Figure 5: Typical Input Diode Forward Voltage vs. Ambient Temperature

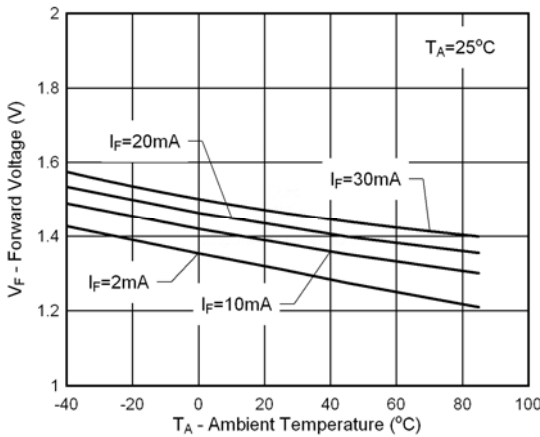


Figure 8: Typical Low Level Output Voltage vs. Ambient Temperature

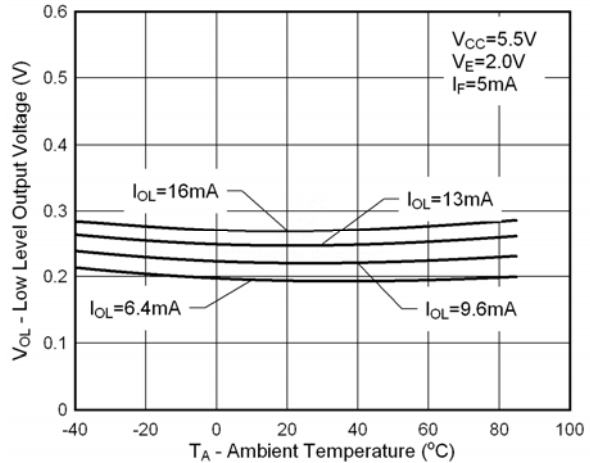


Figure 6: Typical Input Diode Threshold Current vs. Ambient Temperature

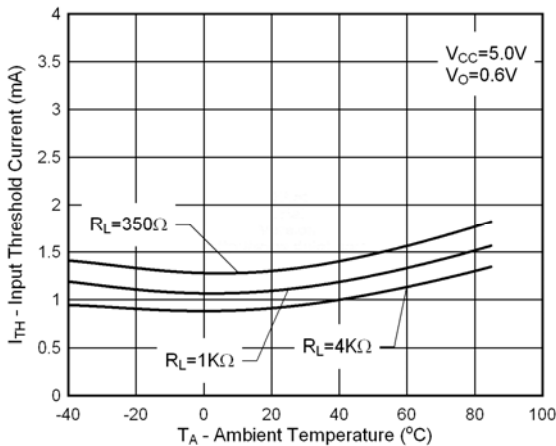
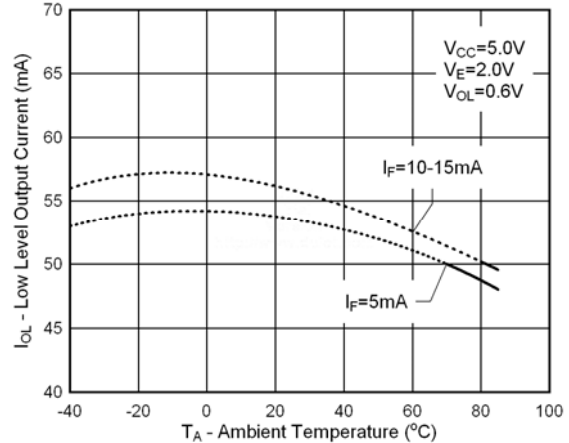


Figure 9: Typical Low Level Output Current vs. Ambient Temperature



### Characteristics Curves

Figure 10: Typical Enable Propagation Delay vs. Ambient Temperature

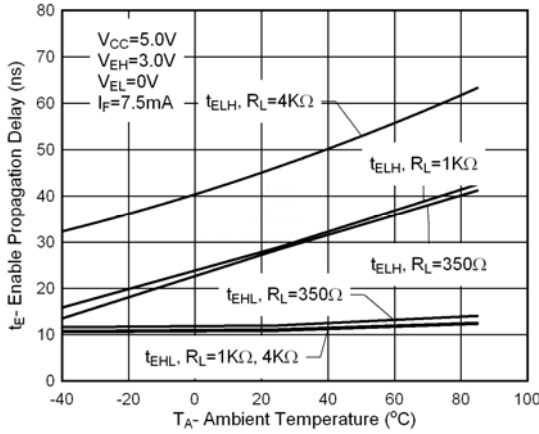


Figure 11: Typical Rise and Fall Time vs. Ambient Temperature

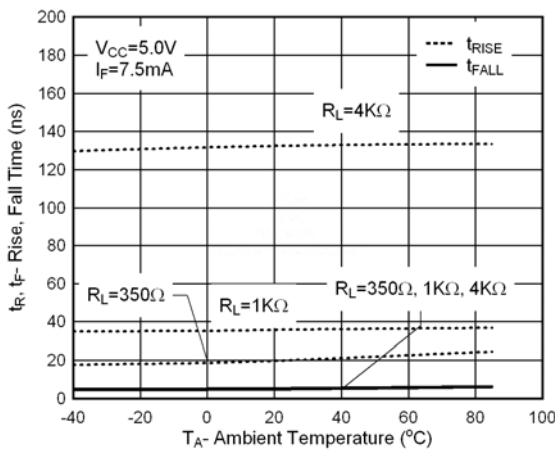


Figure 12: Typical Propagation Delay vs. Ambient

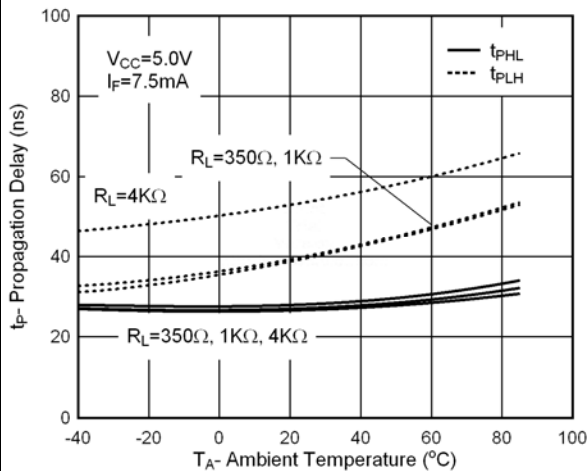


Figure 13: Typical Propagation Delay vs. Input Forward Current

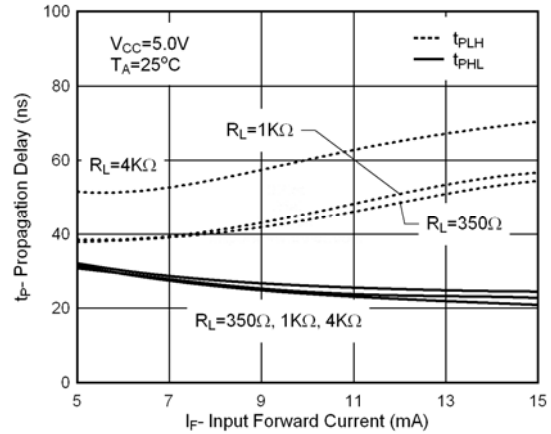


Figure 14: Typical Pulse Width Distortion vs. Input Forward Current

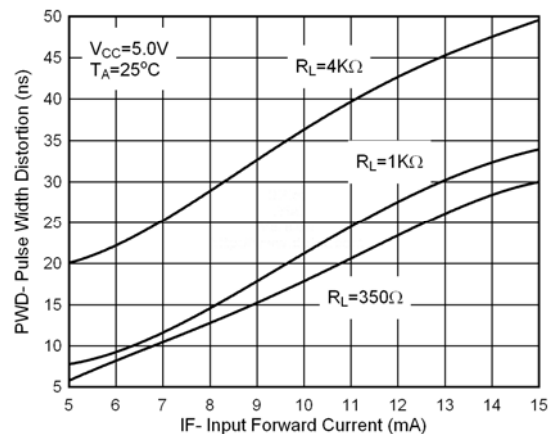
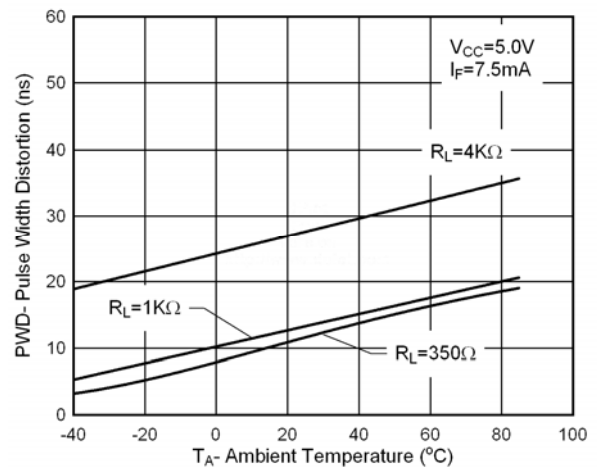


Figure 15: Typical Pulse Width Distortion vs. Ambient Temperature



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